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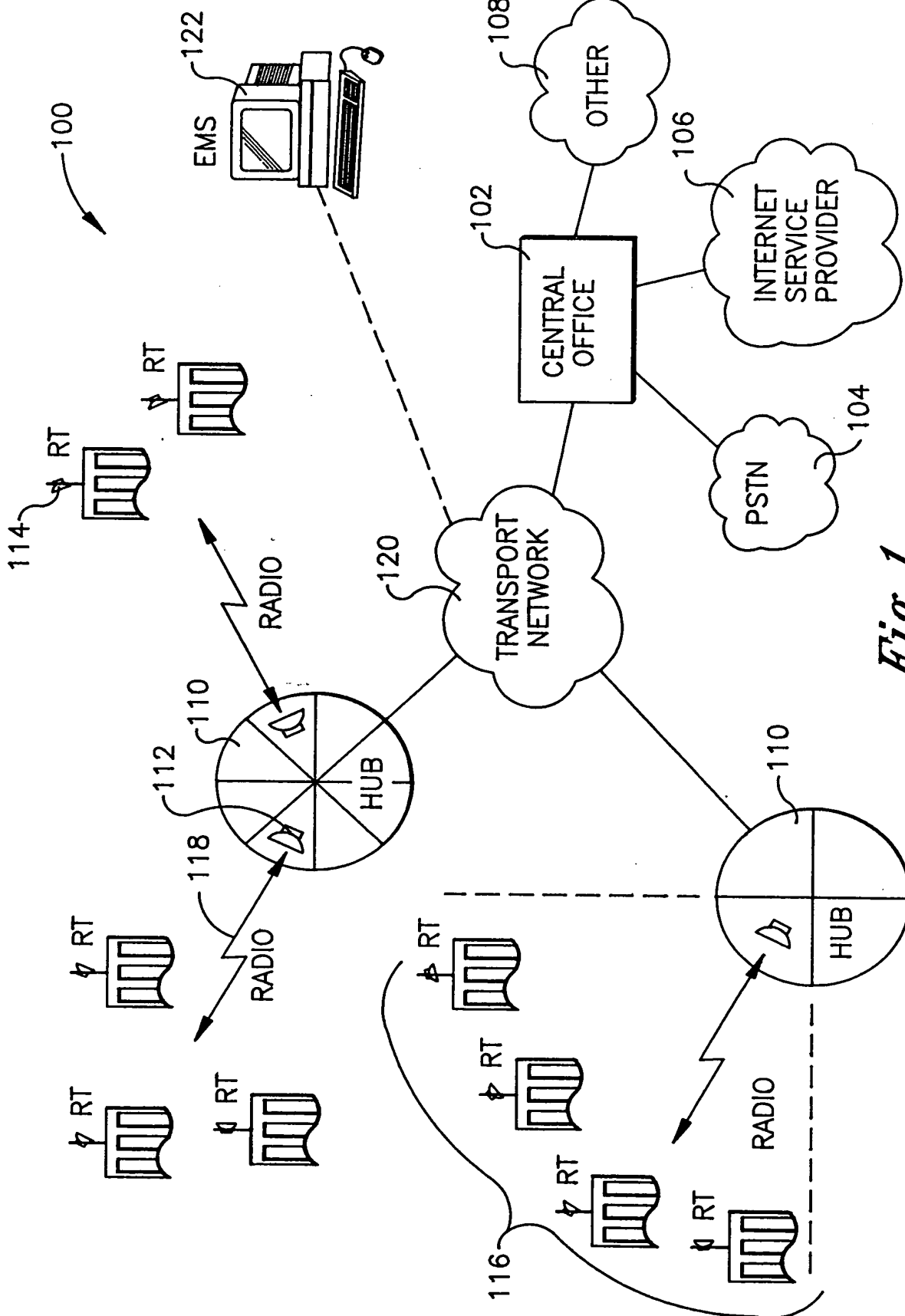
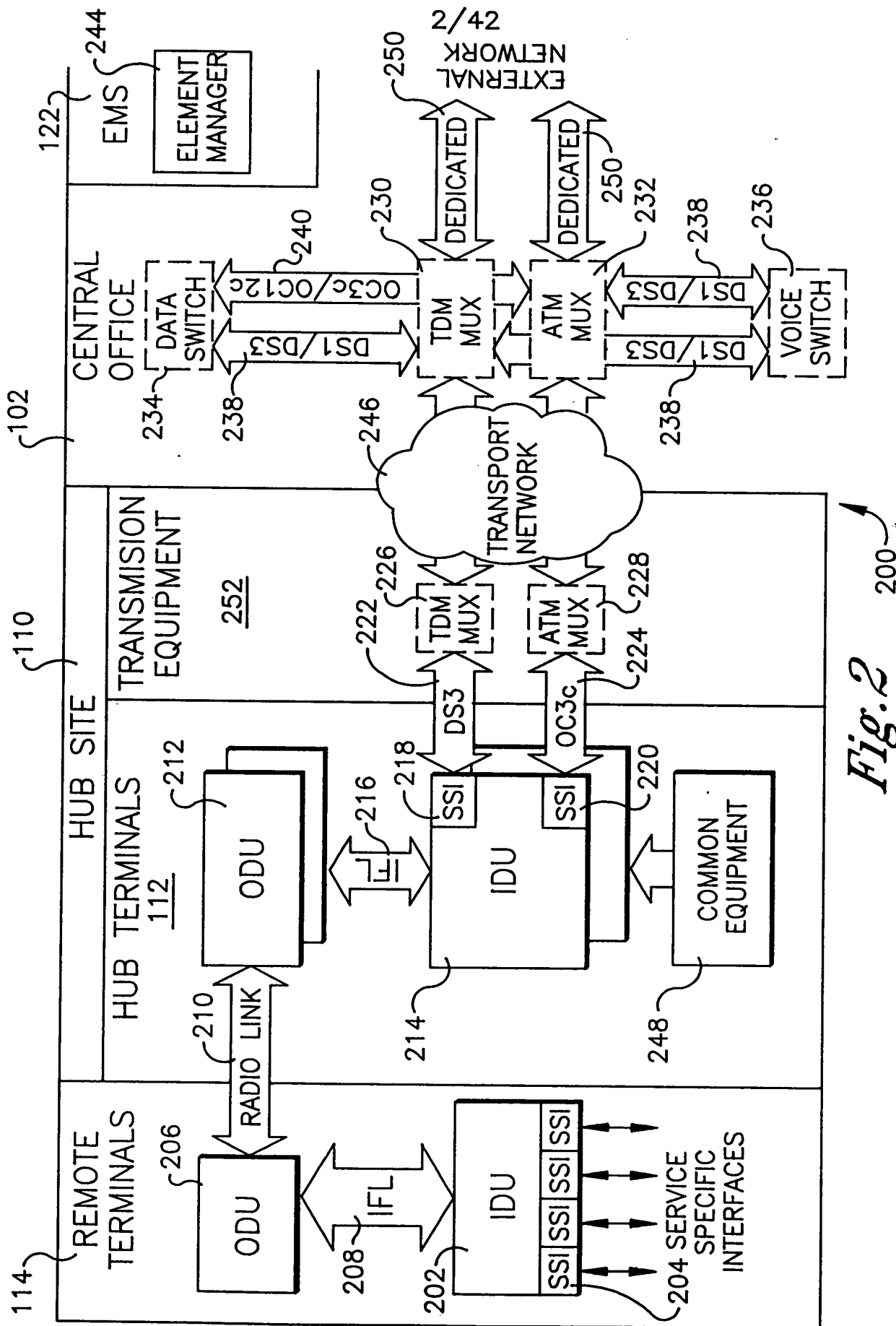


Fig. 1



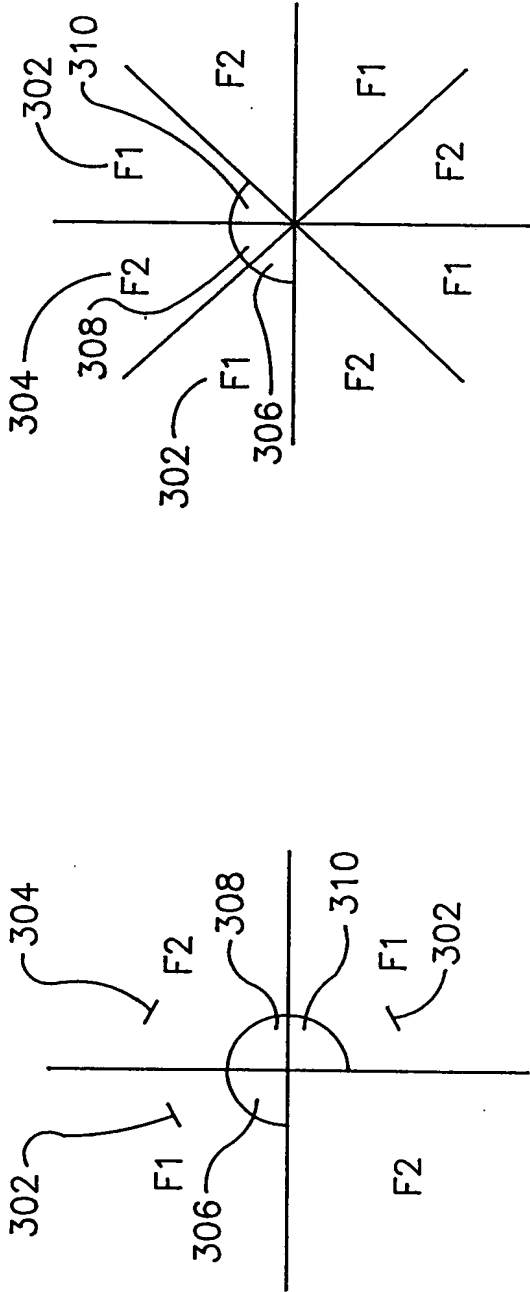


Fig. 3A

Fig. 3B

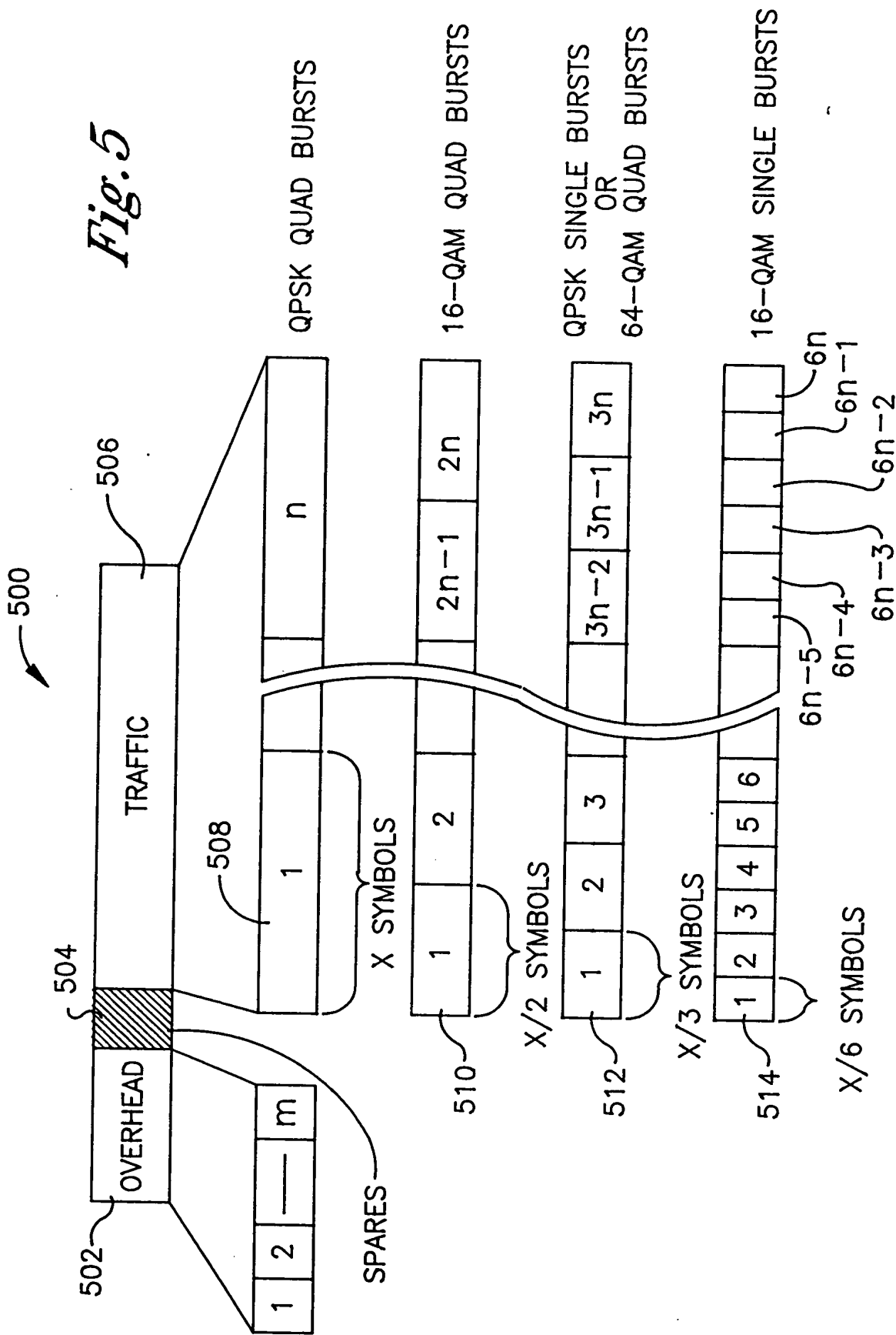


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FRAME 1	FRAME 2	FRAME 3		FRAME N-1	FRAME N
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Fig. 4

**Fig. 5**



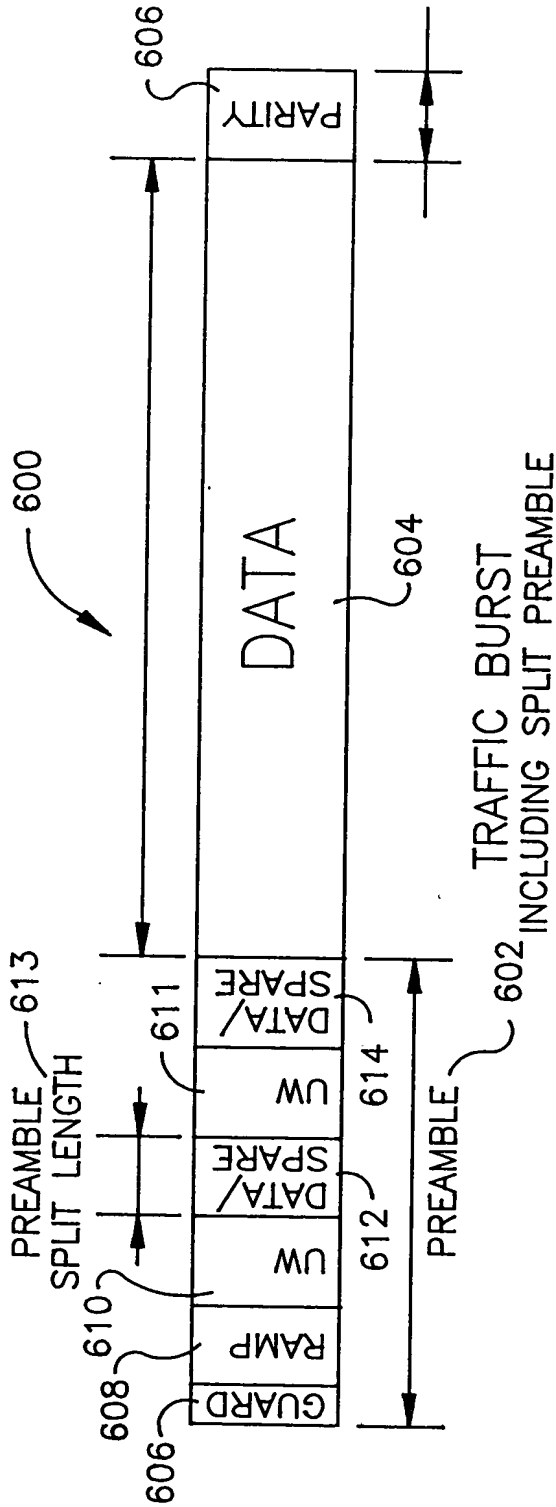


Fig. 6

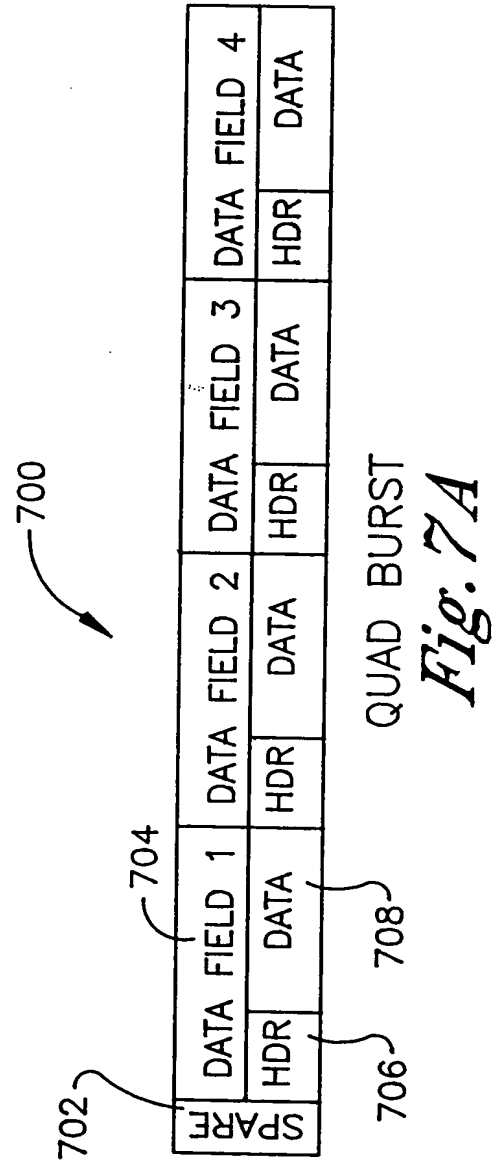


Fig. 7A

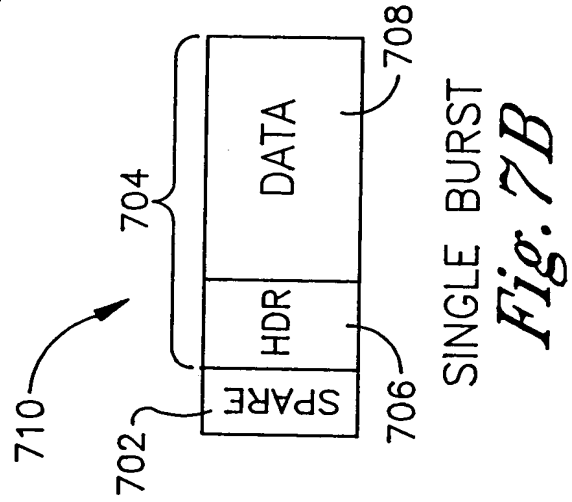


Fig. 7B

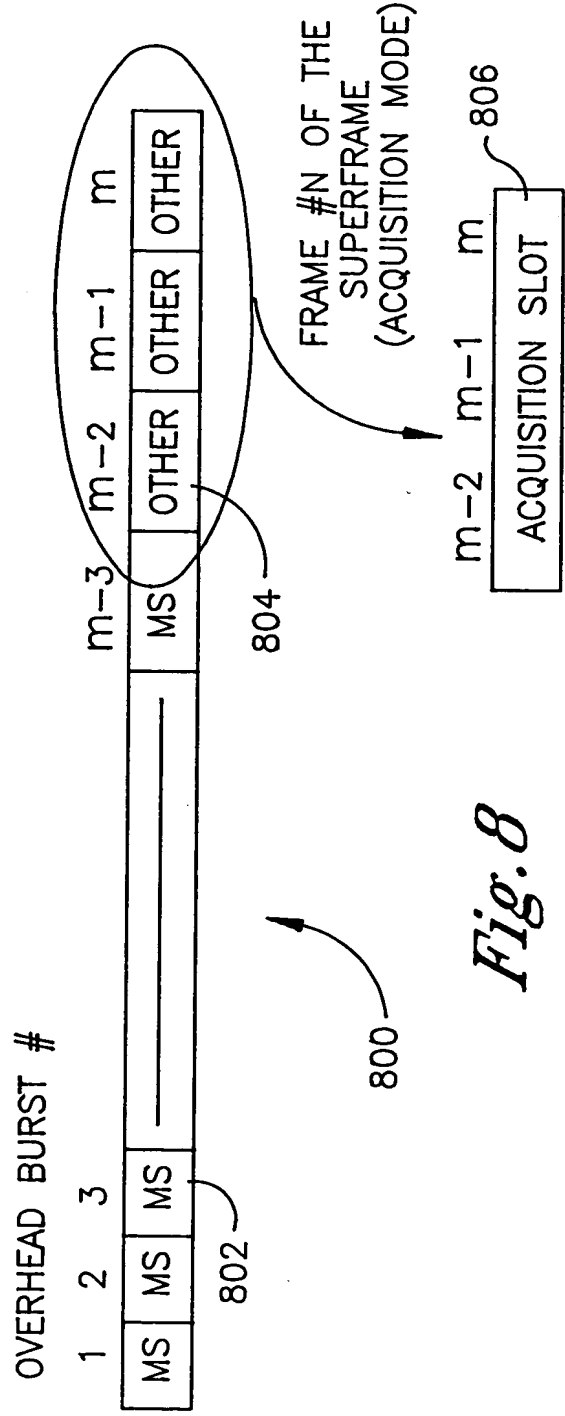


Fig. 8

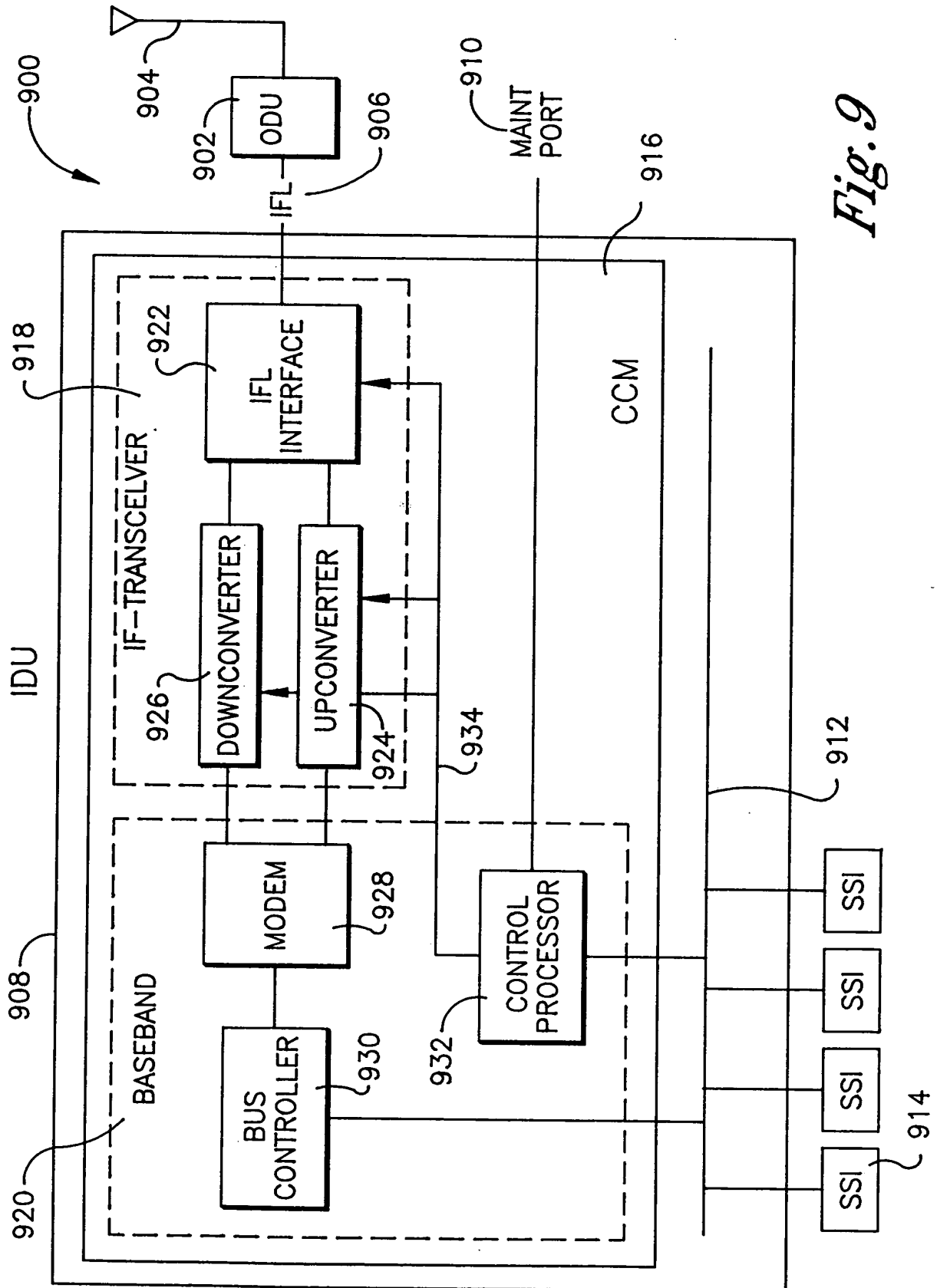


Fig. 9

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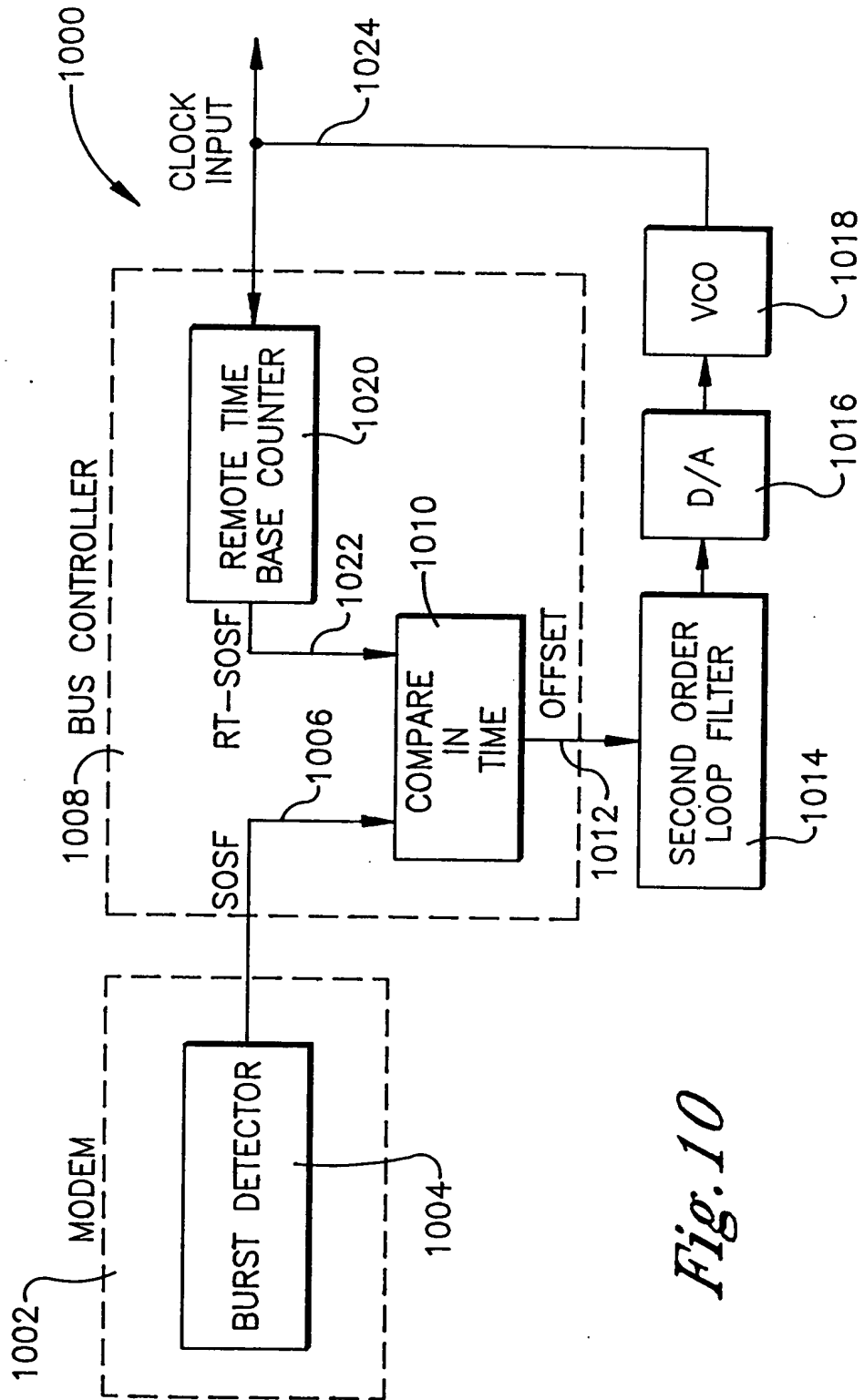
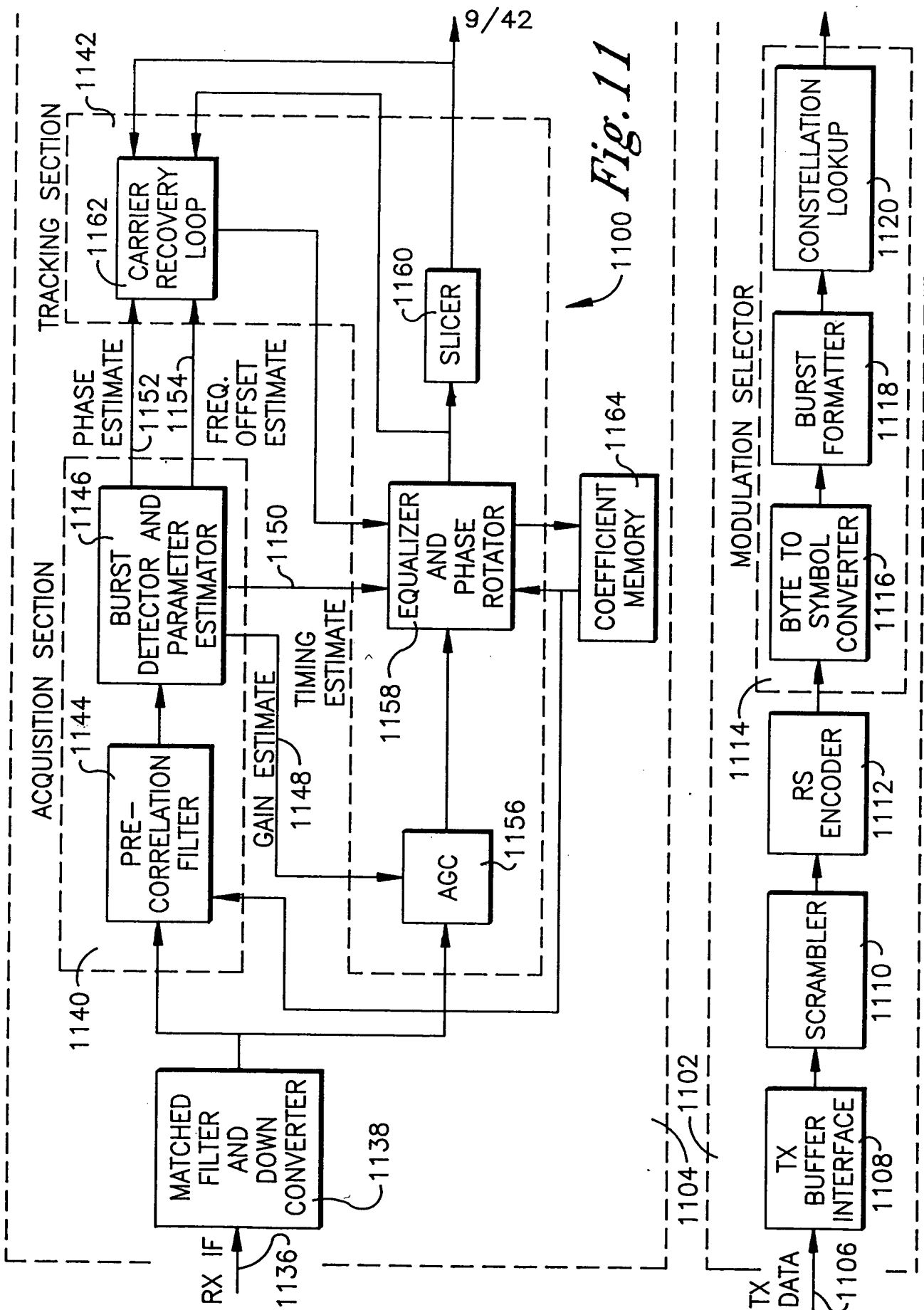


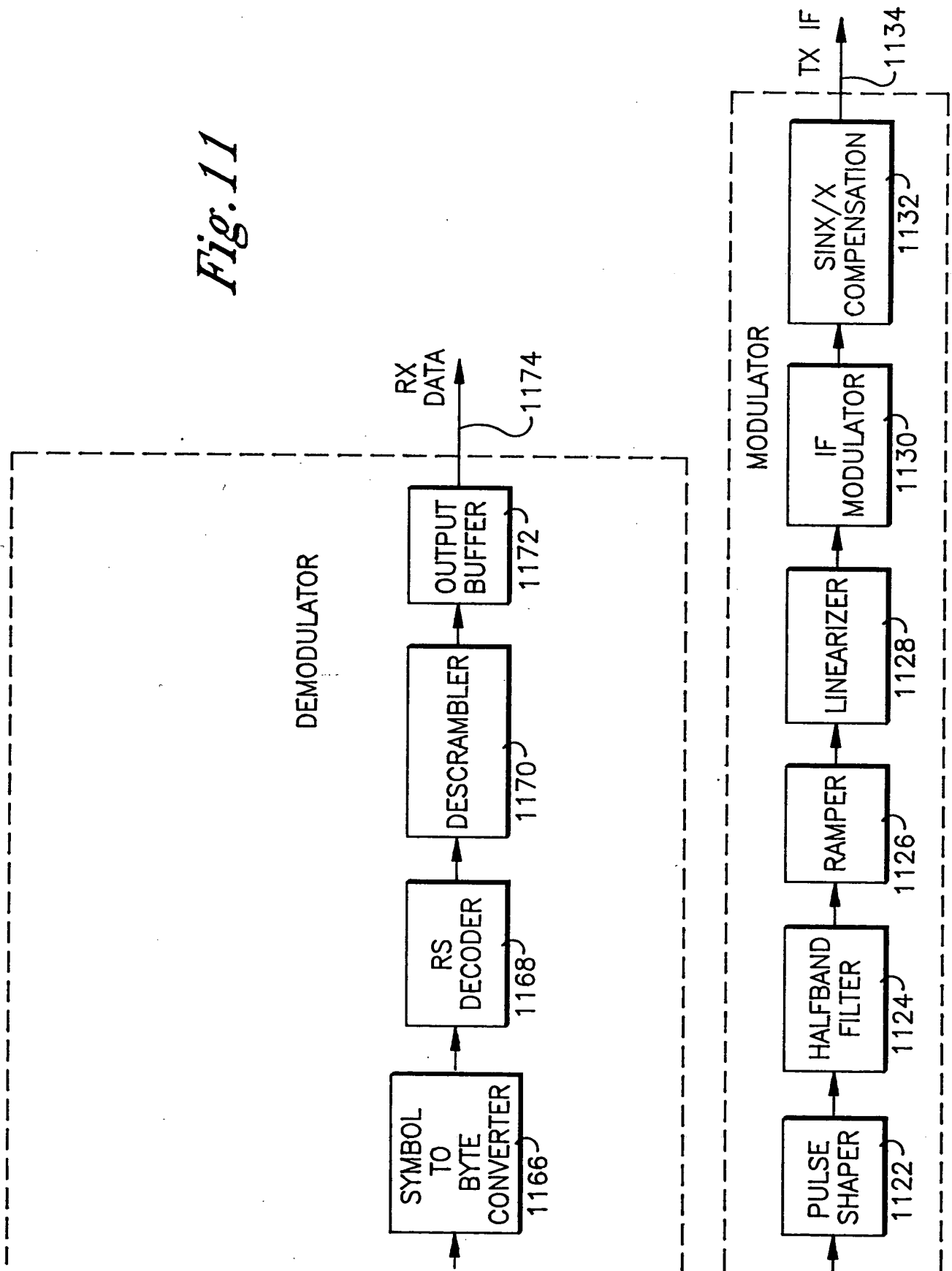
Fig. 10



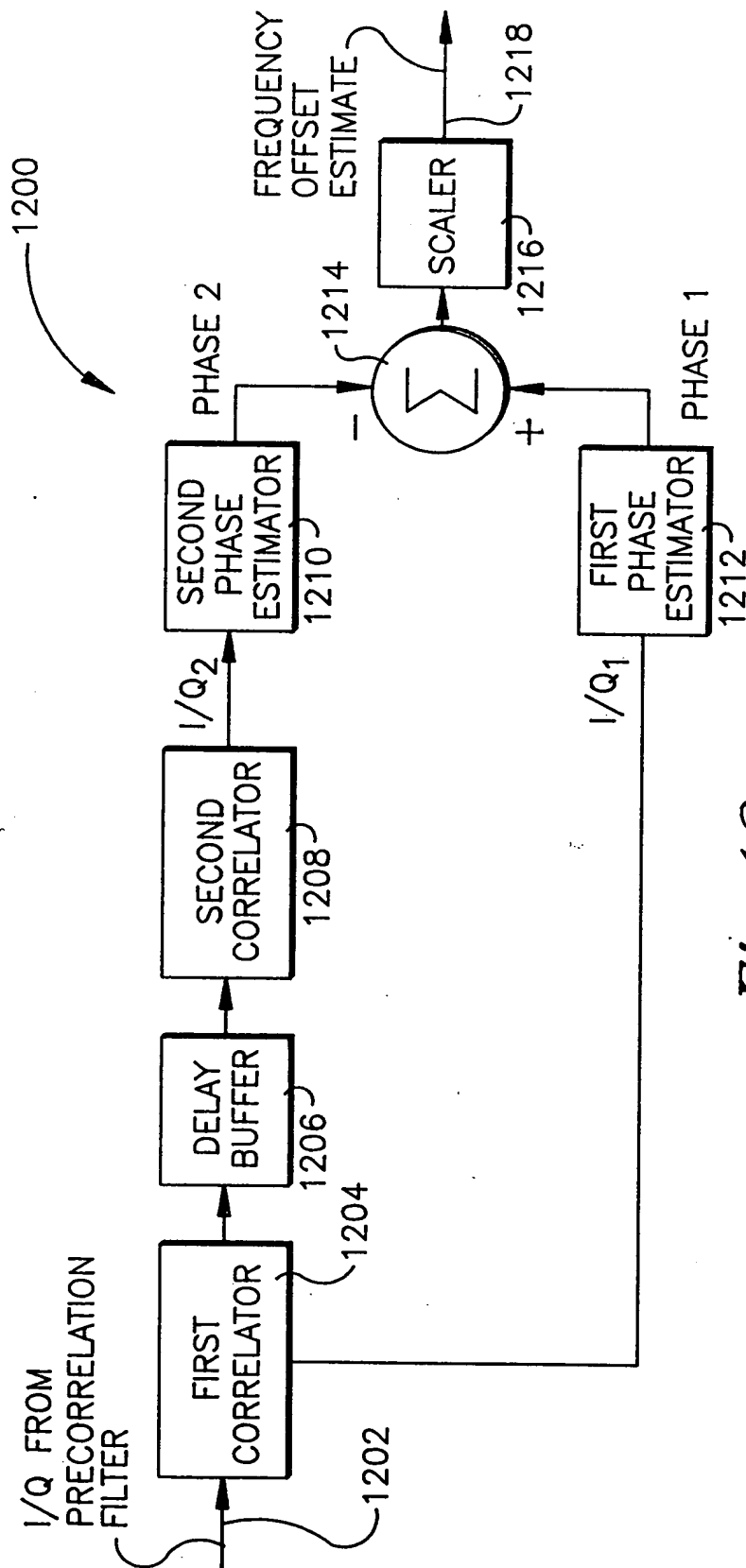


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*Fig. 11*



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*Fig. 12*

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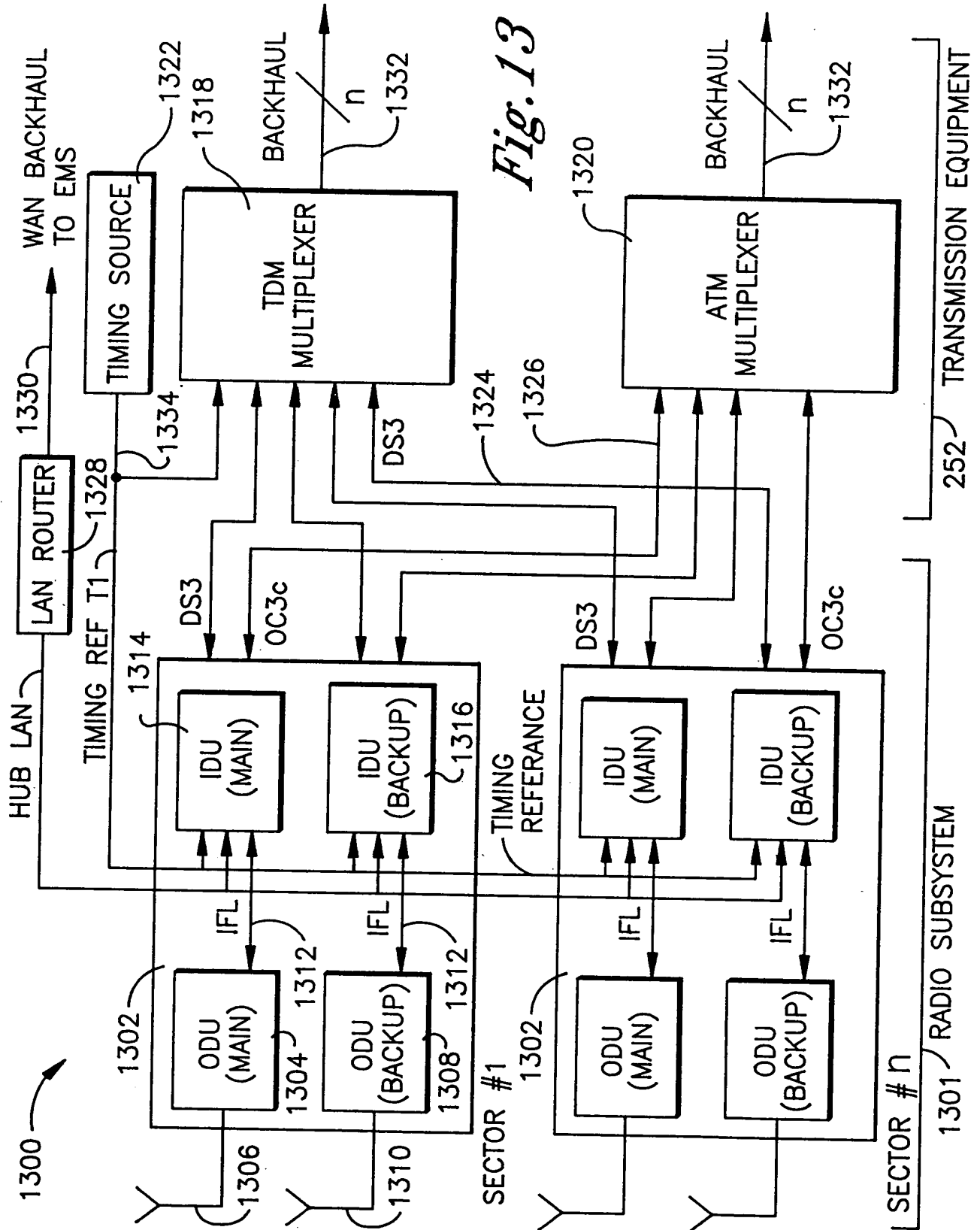


Fig. 13

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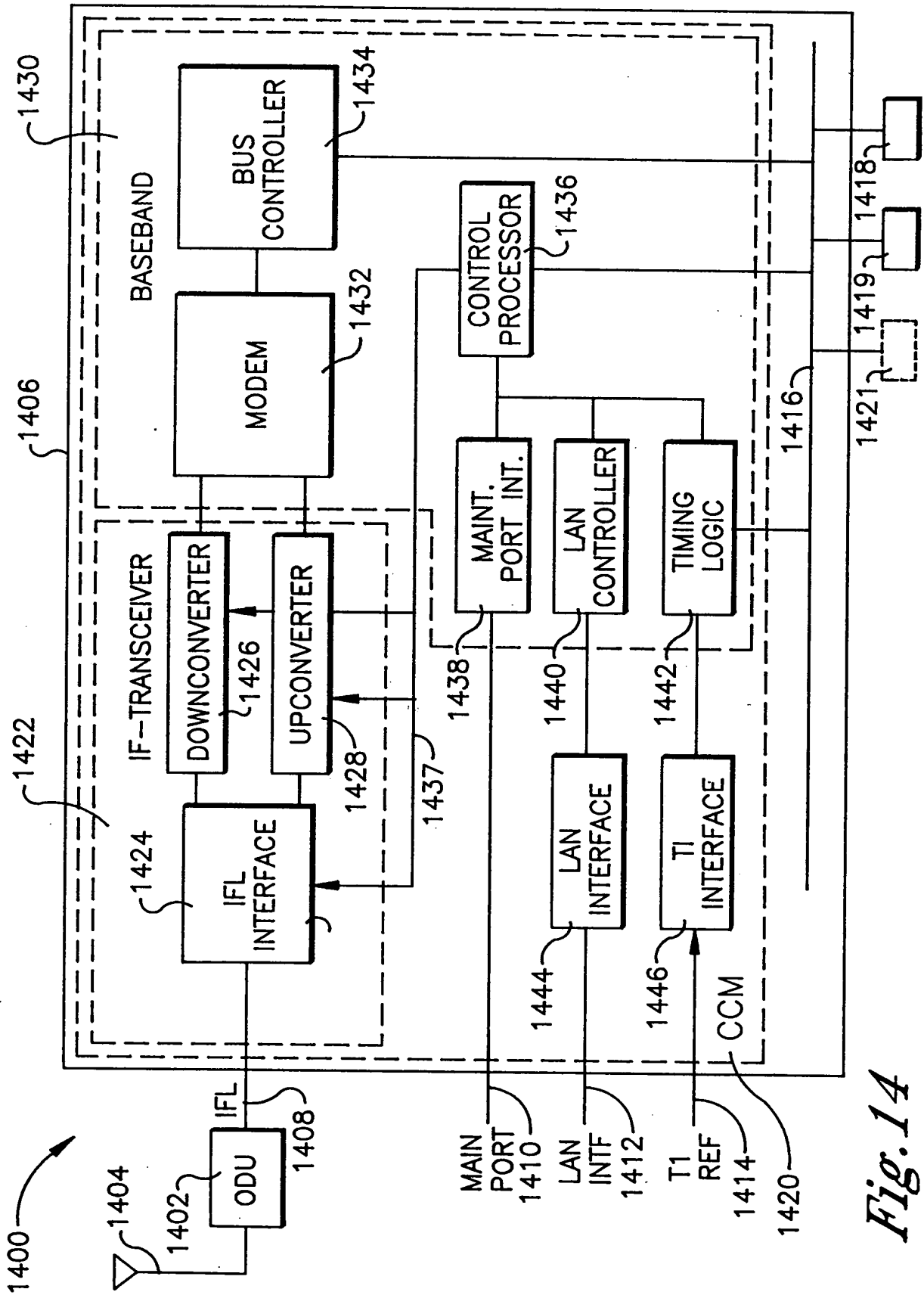
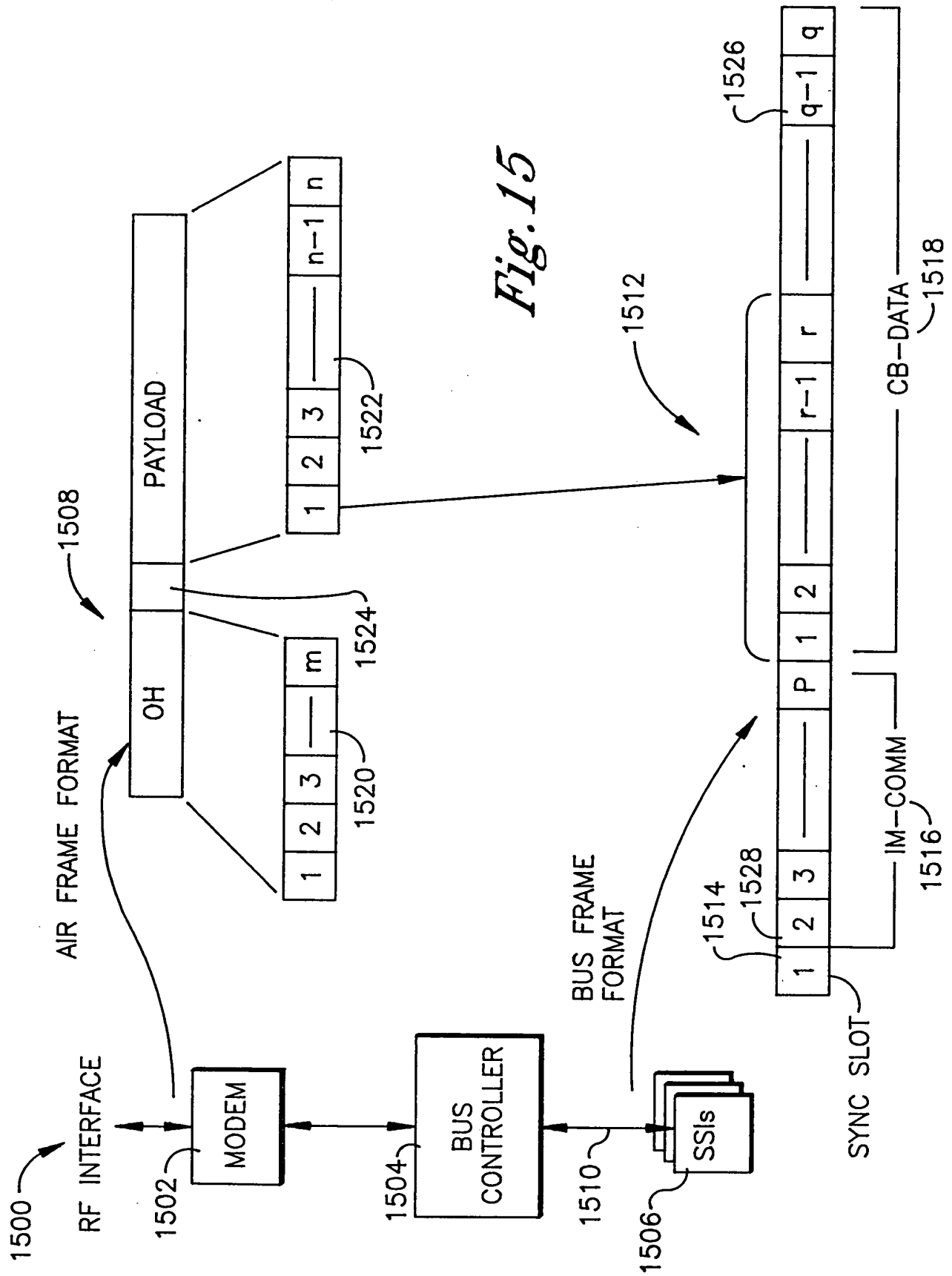


Fig. 14



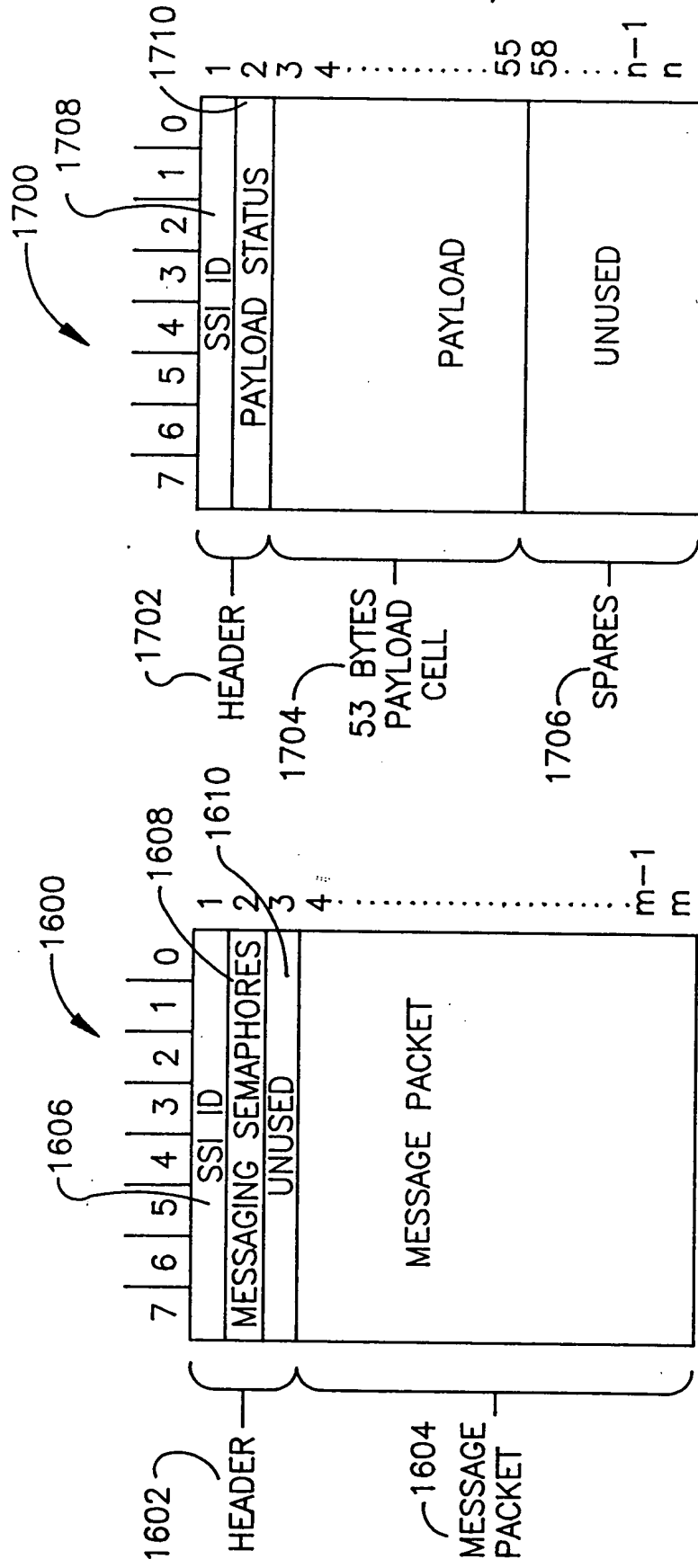
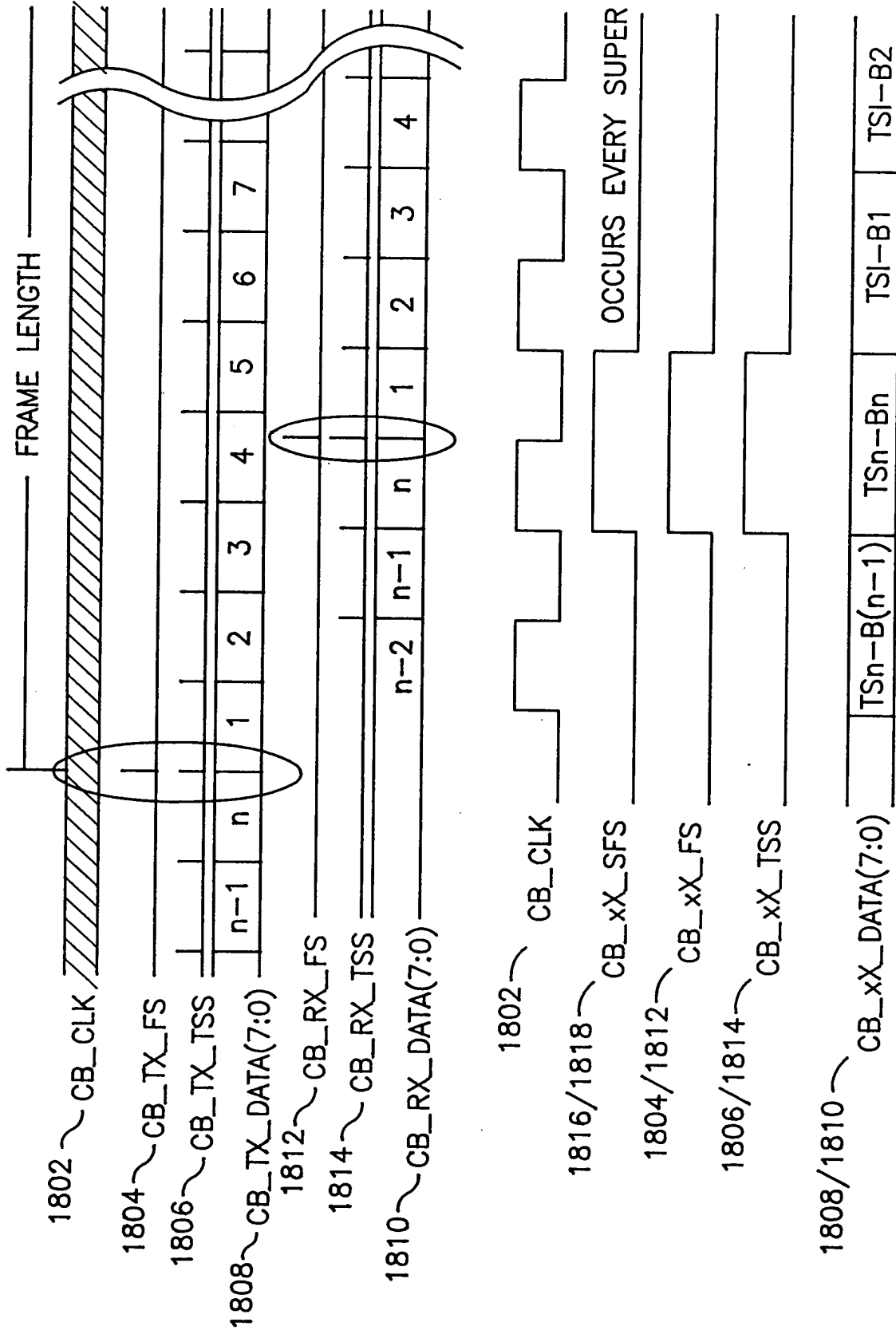


Fig. 16

Fig. 17

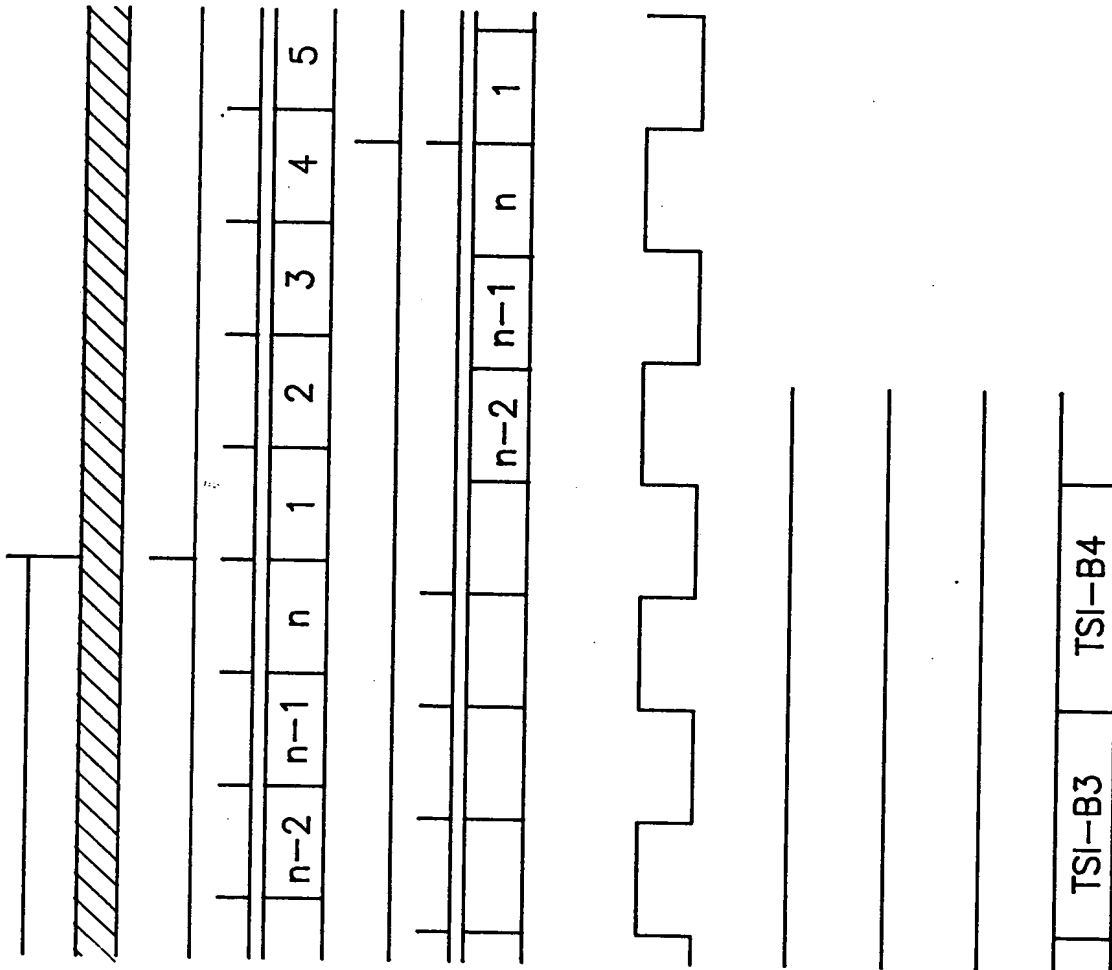


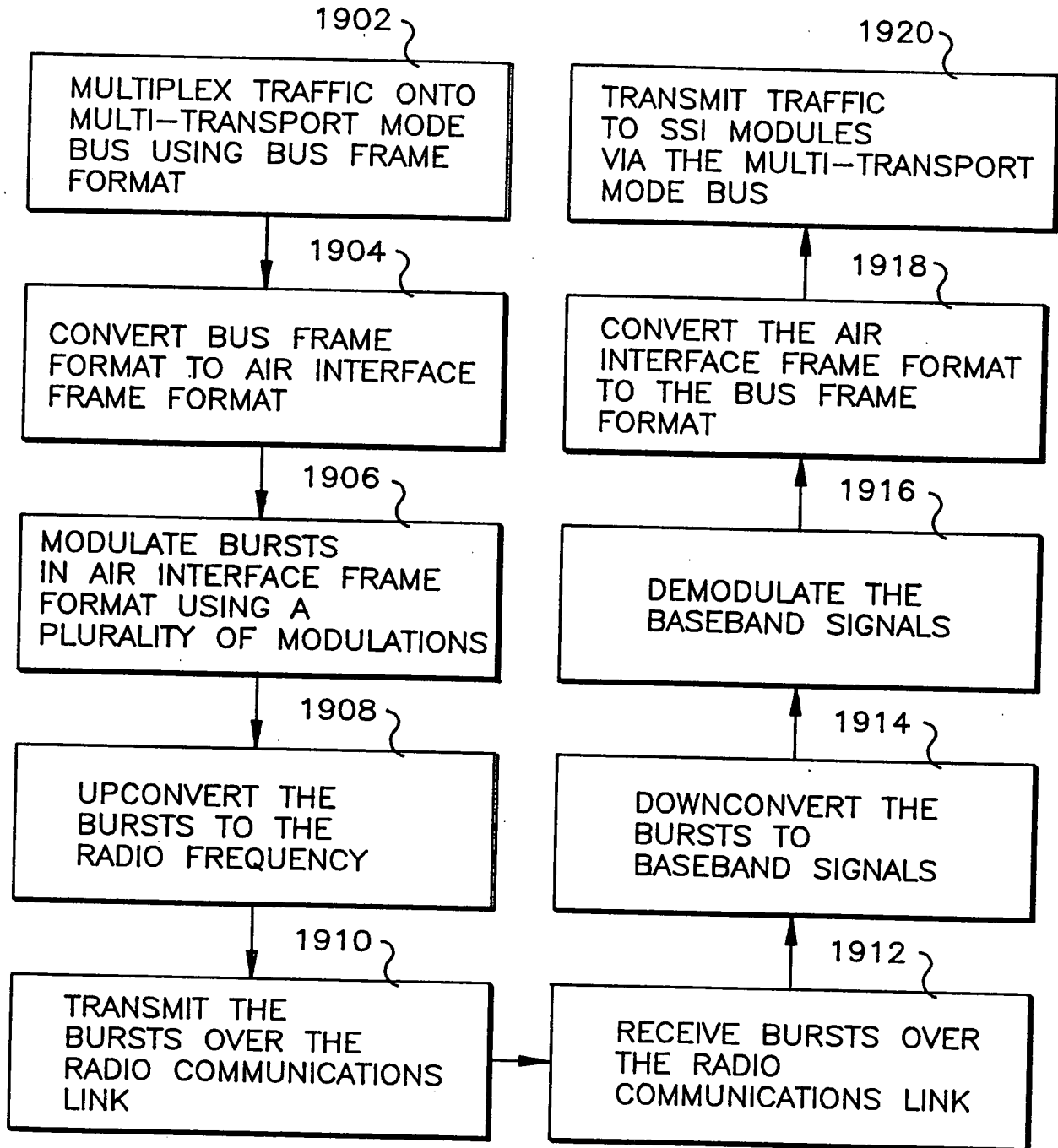
**Fig. 18** CELL BUS TIMING



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*Fig. 18*





*Fig. 19*

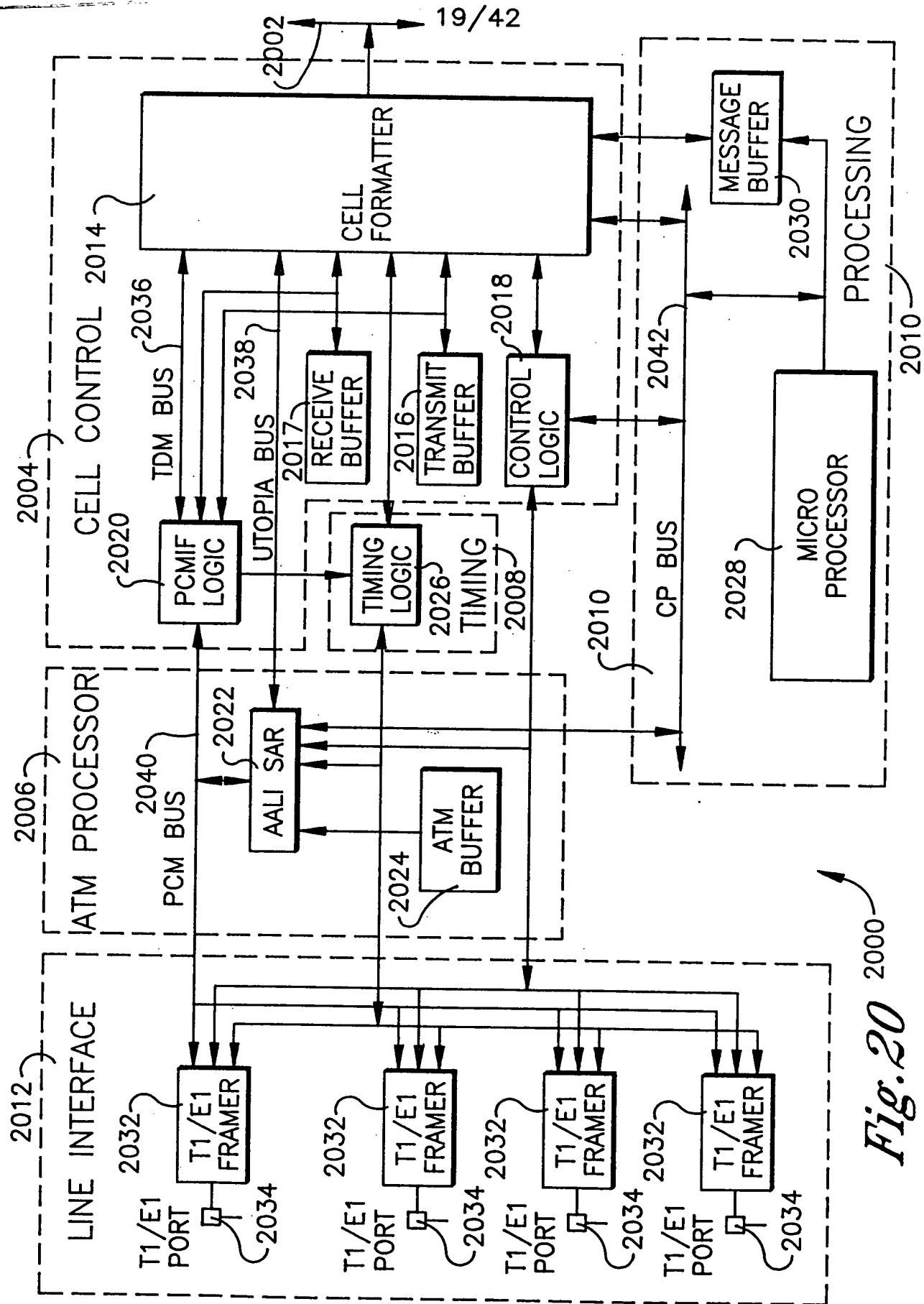


Fig. 20

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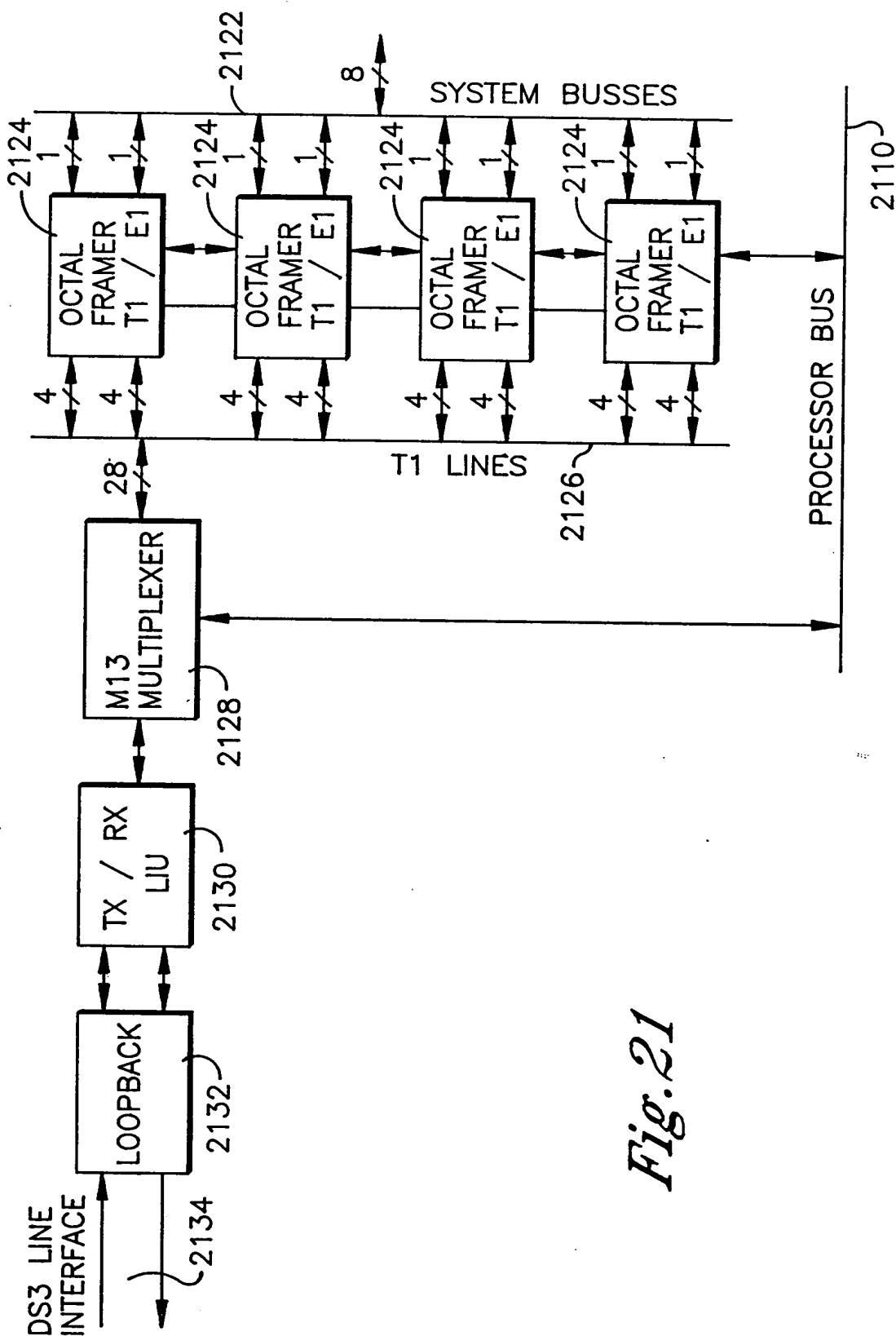
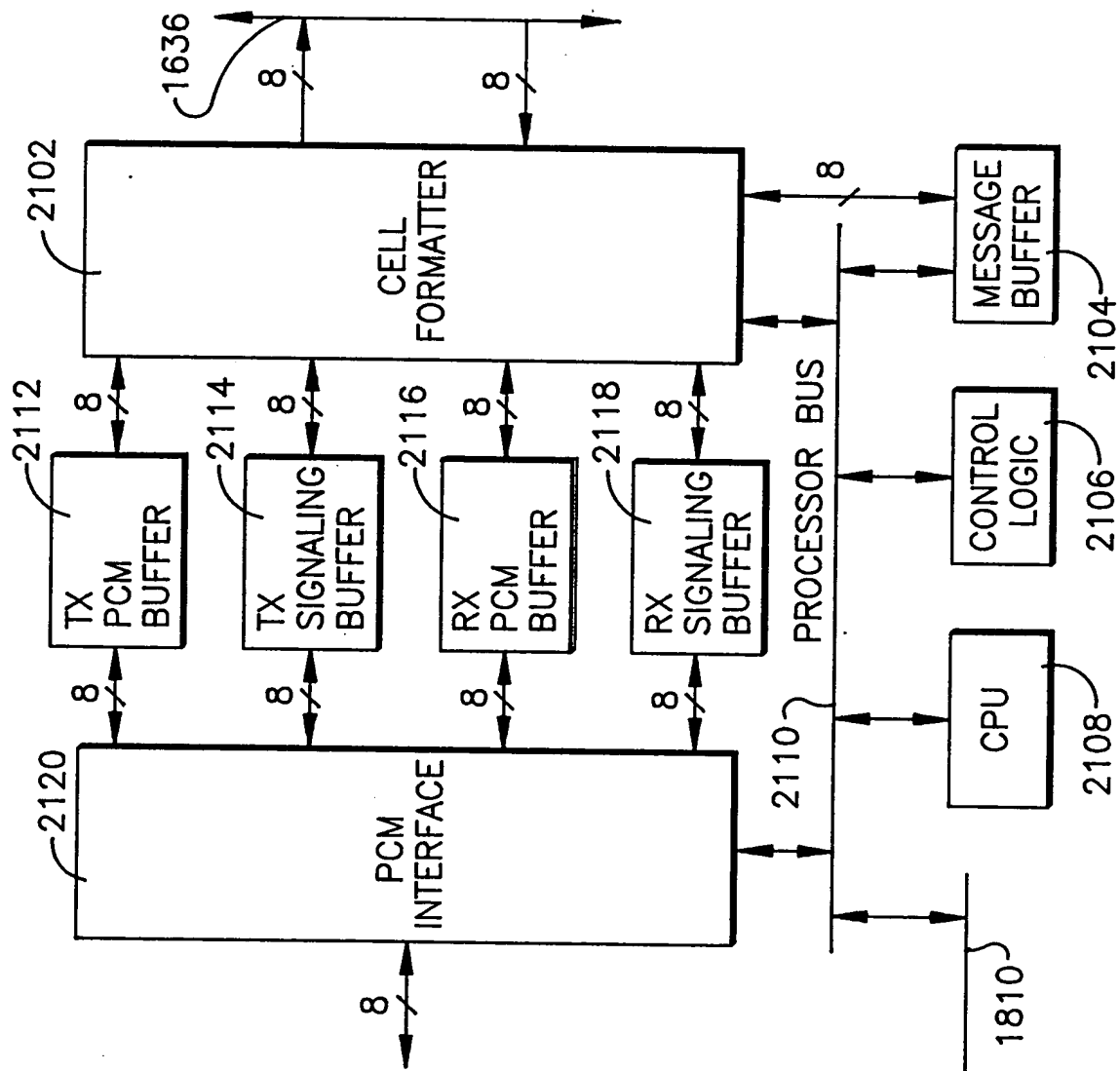


Fig. 21

Fig. 21



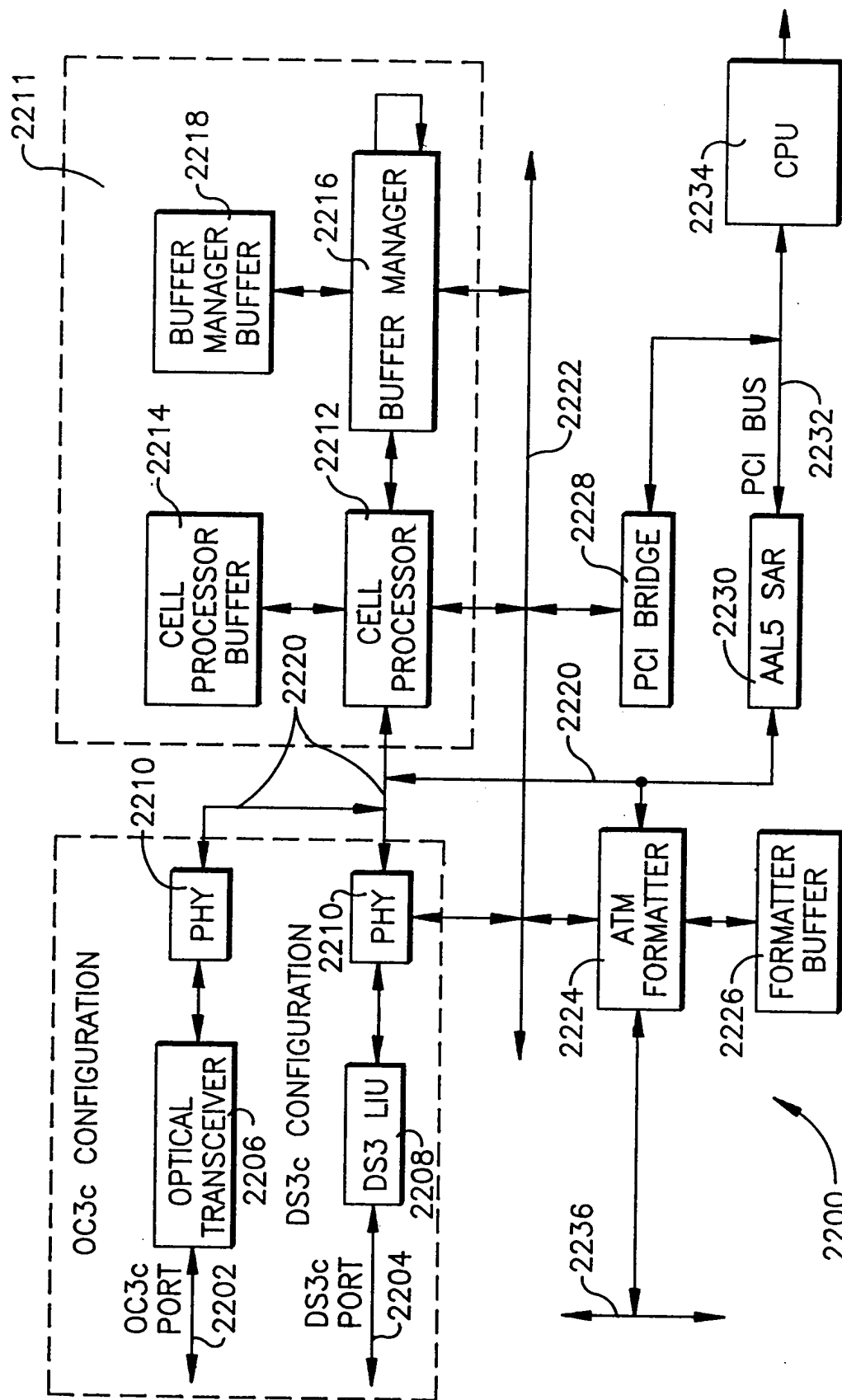


Fig. 22

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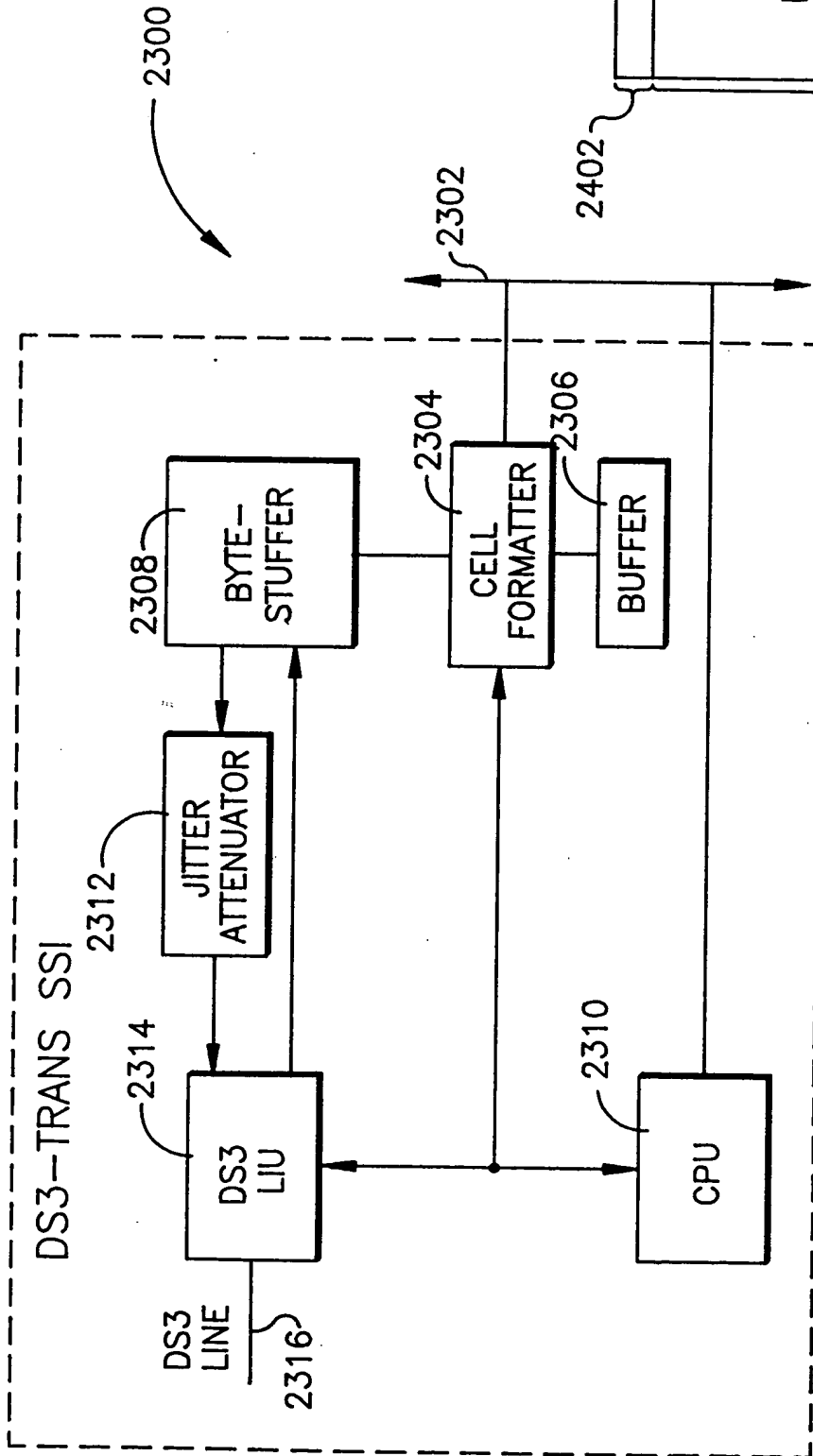


Fig. 23

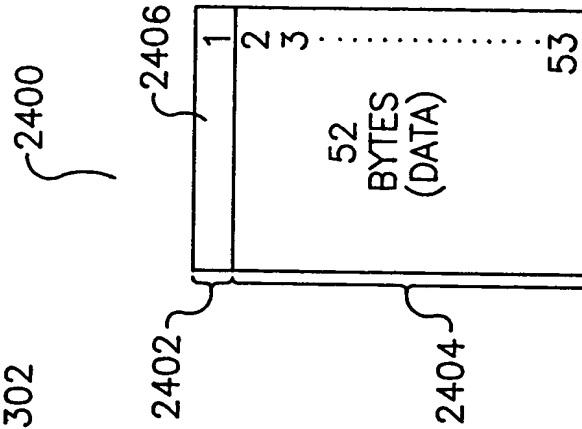


Fig. 24

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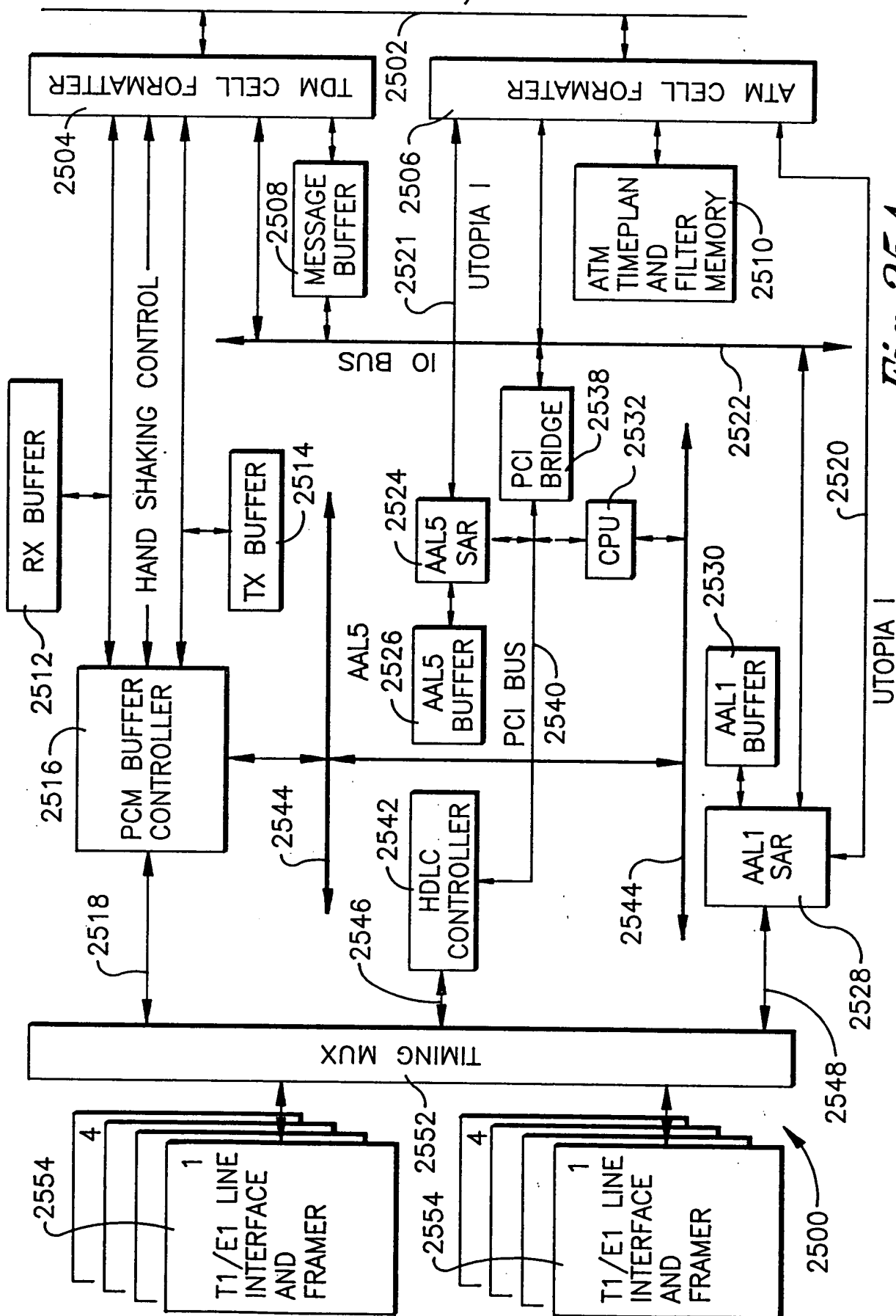


Fig. 25A



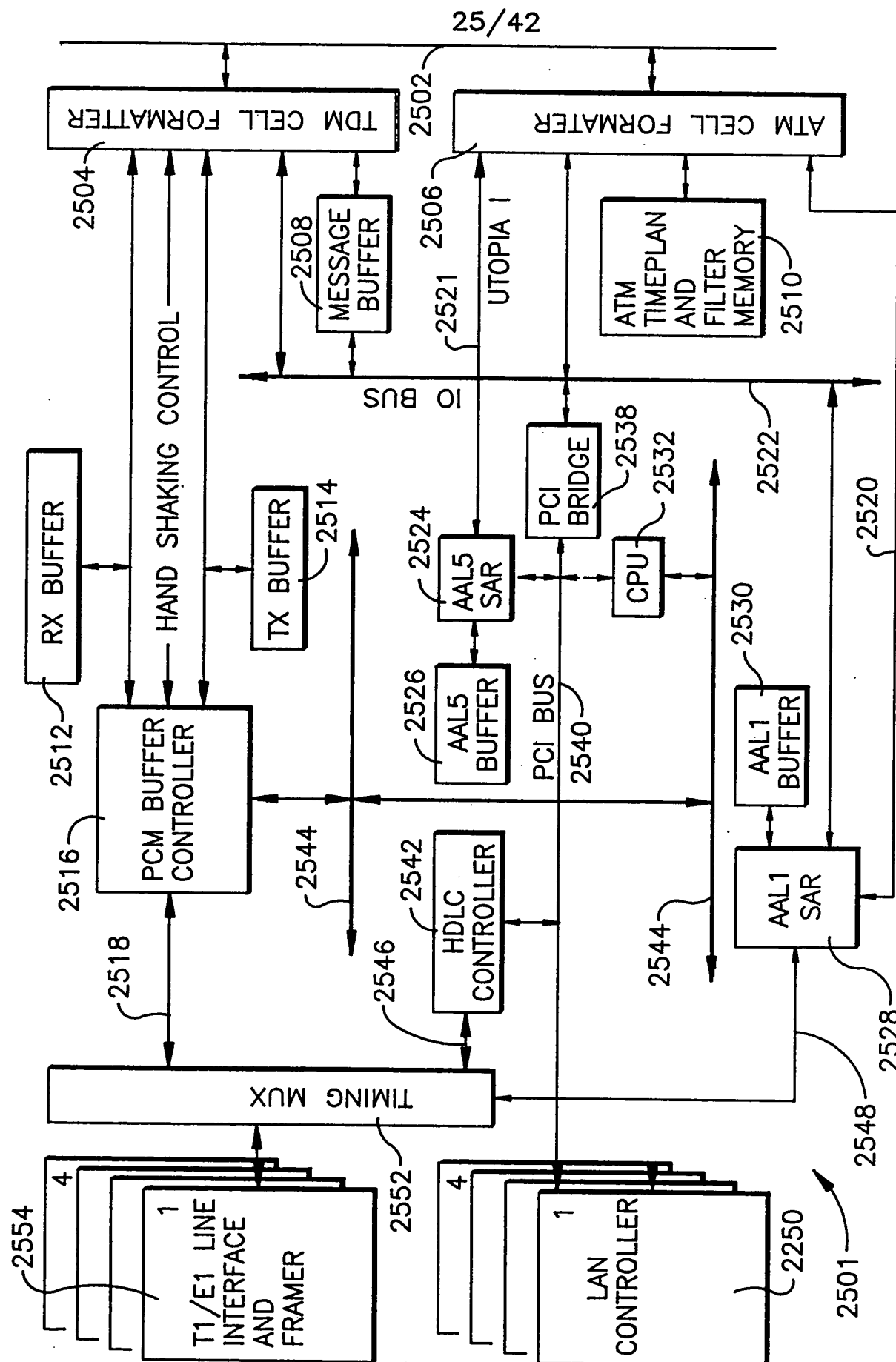
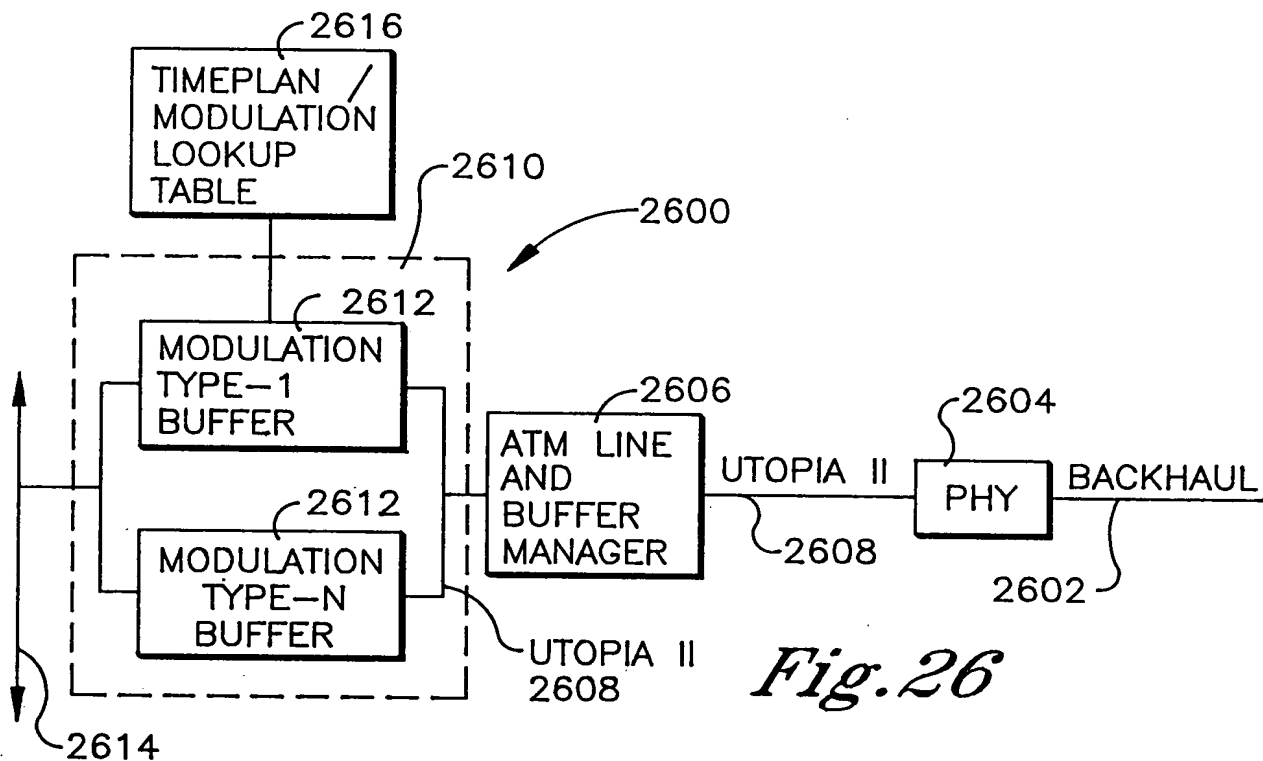
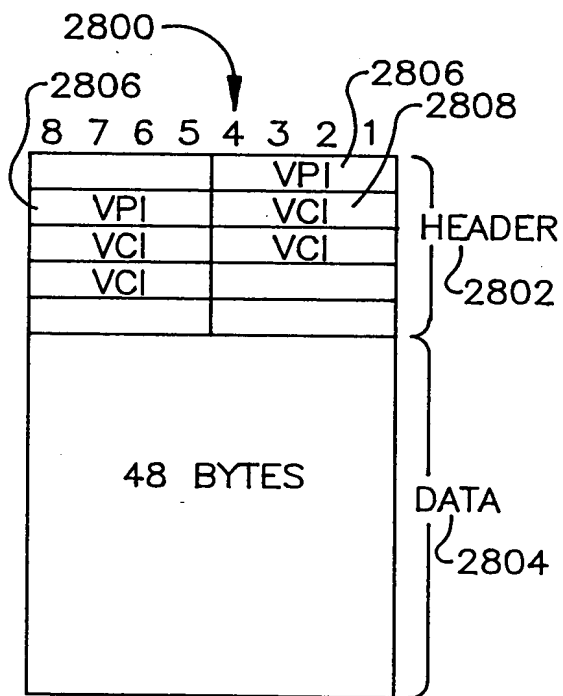


Fig. 25B

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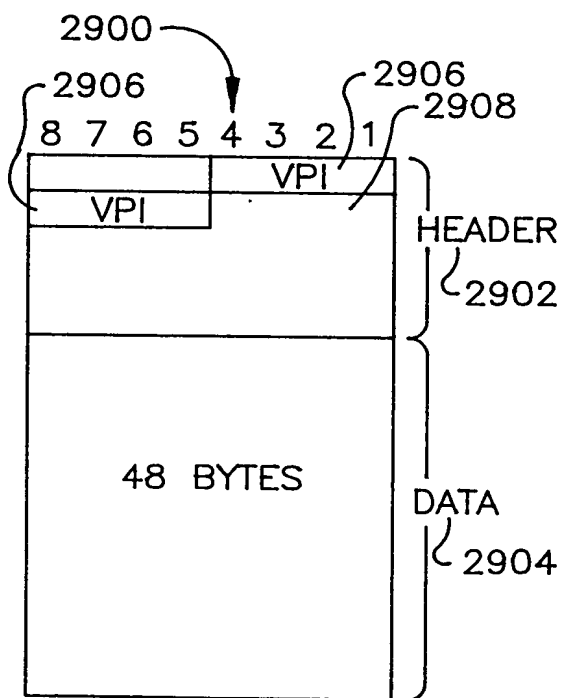


*Fig. 26*



ATM CELL

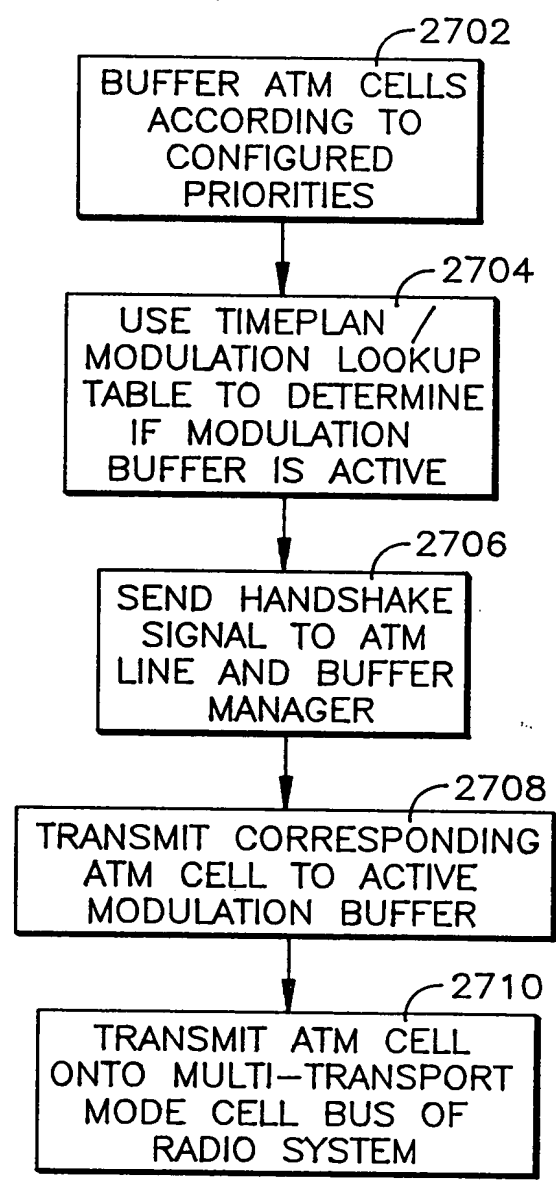
*Fig. 28*



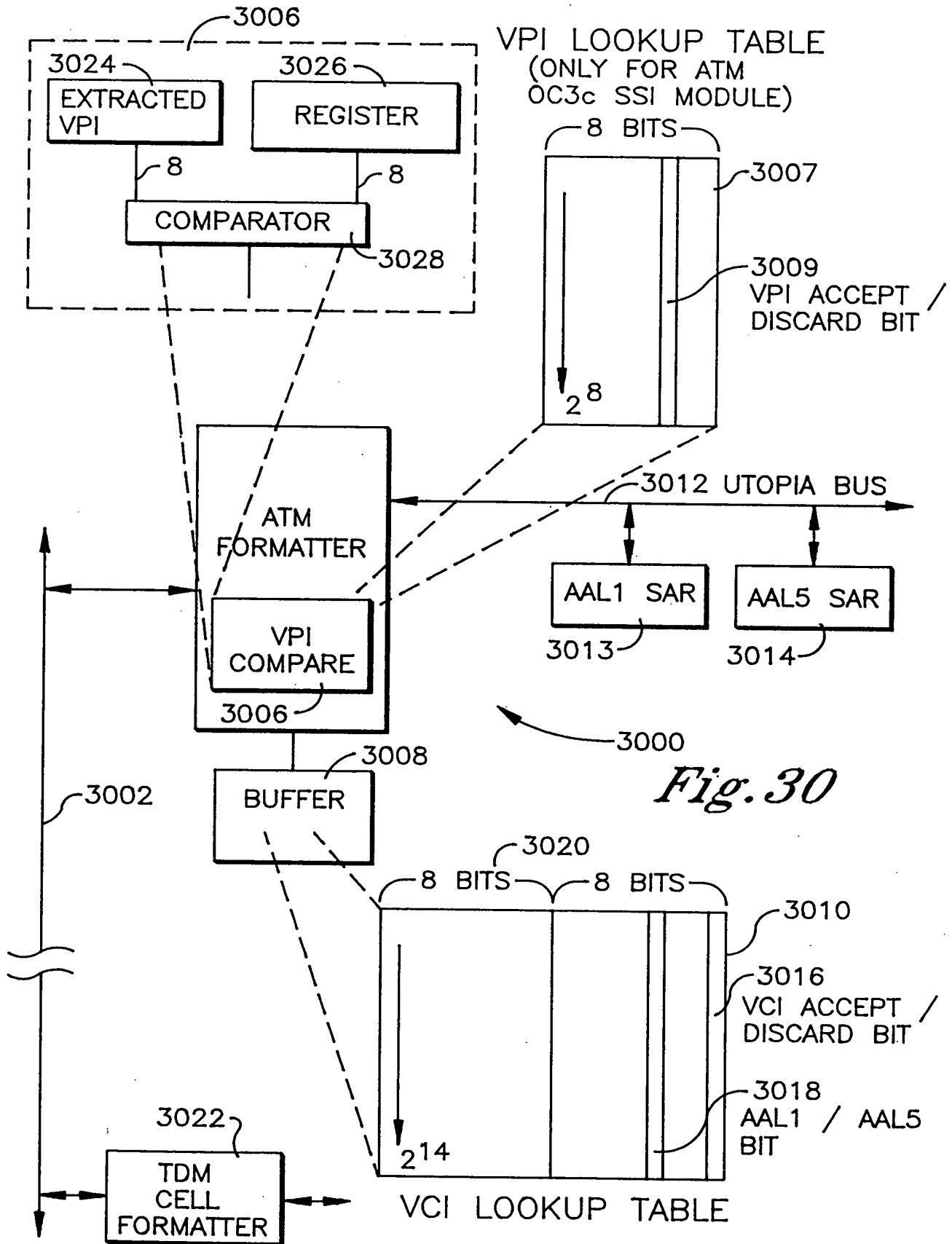
TDM CELL

*Fig. 29*

Fig. 27

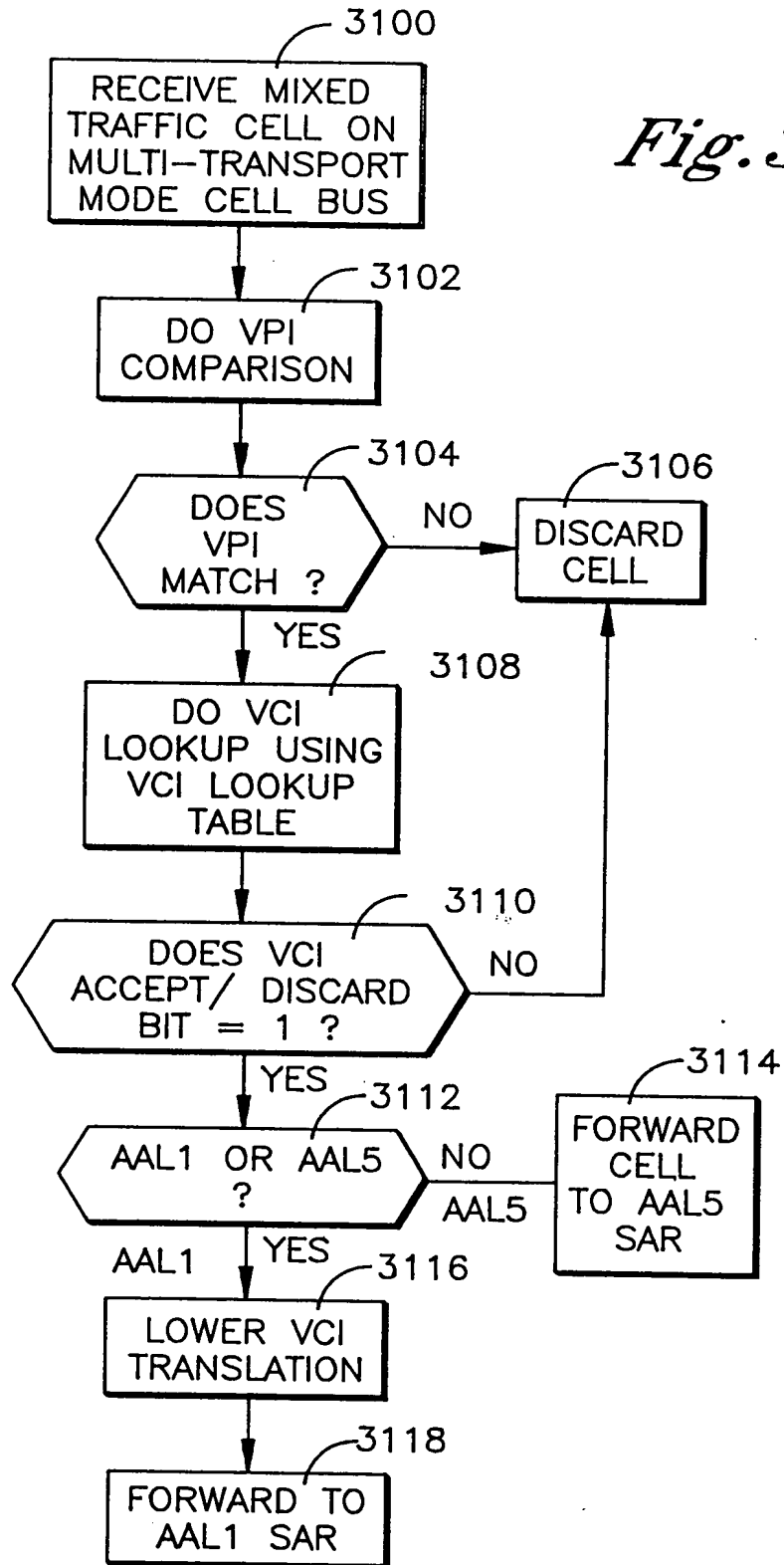


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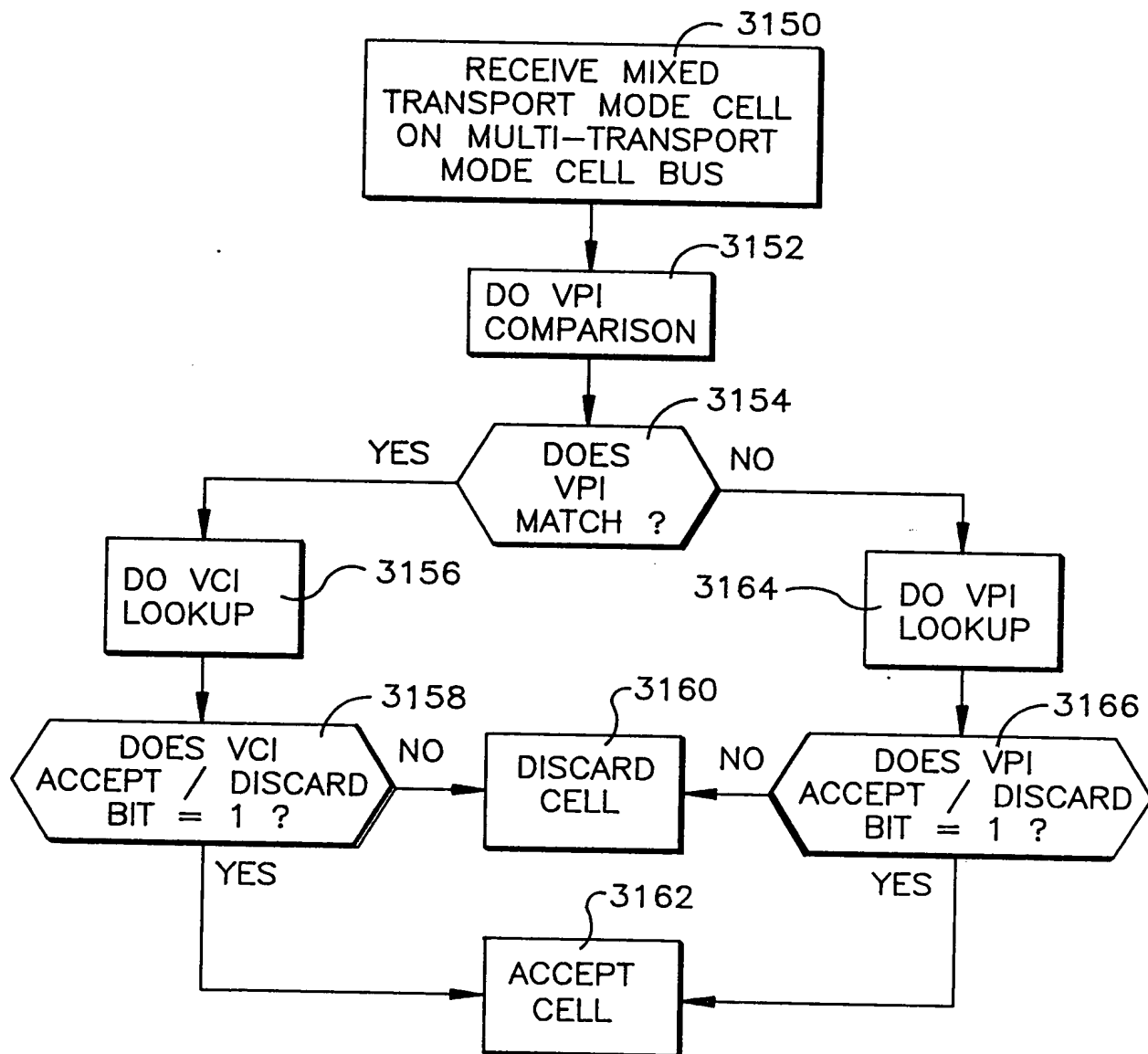
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*Fig. 31A*

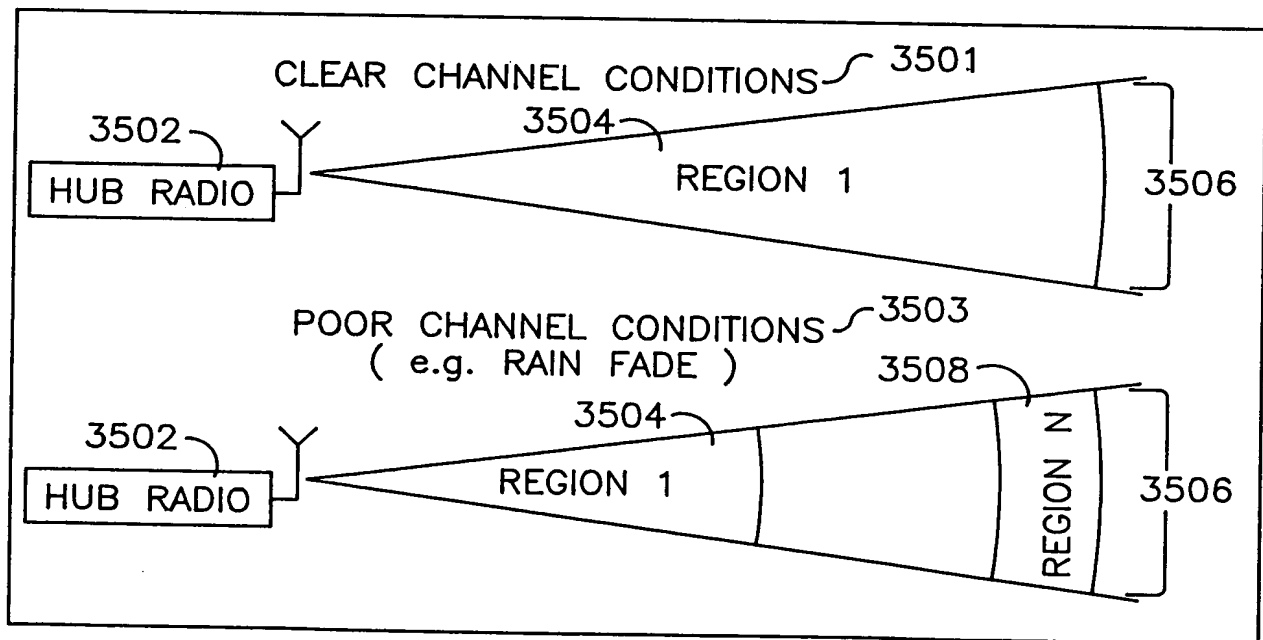
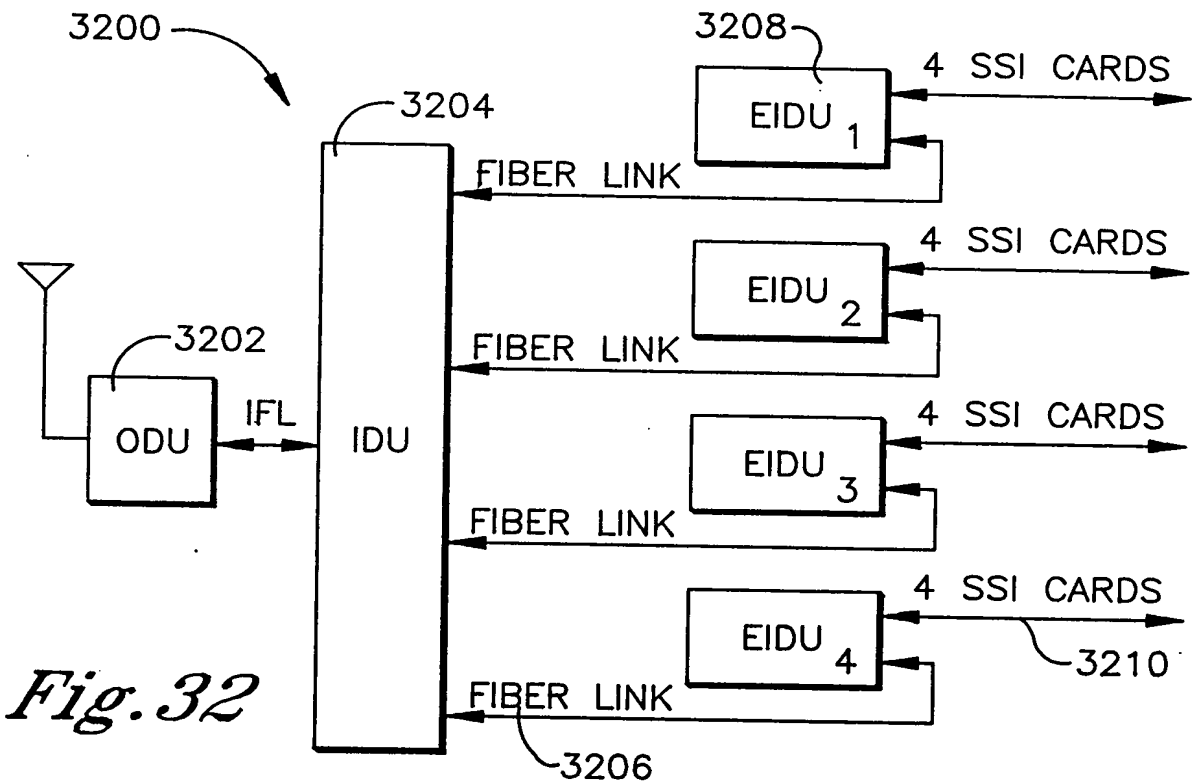


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Fig. 31B



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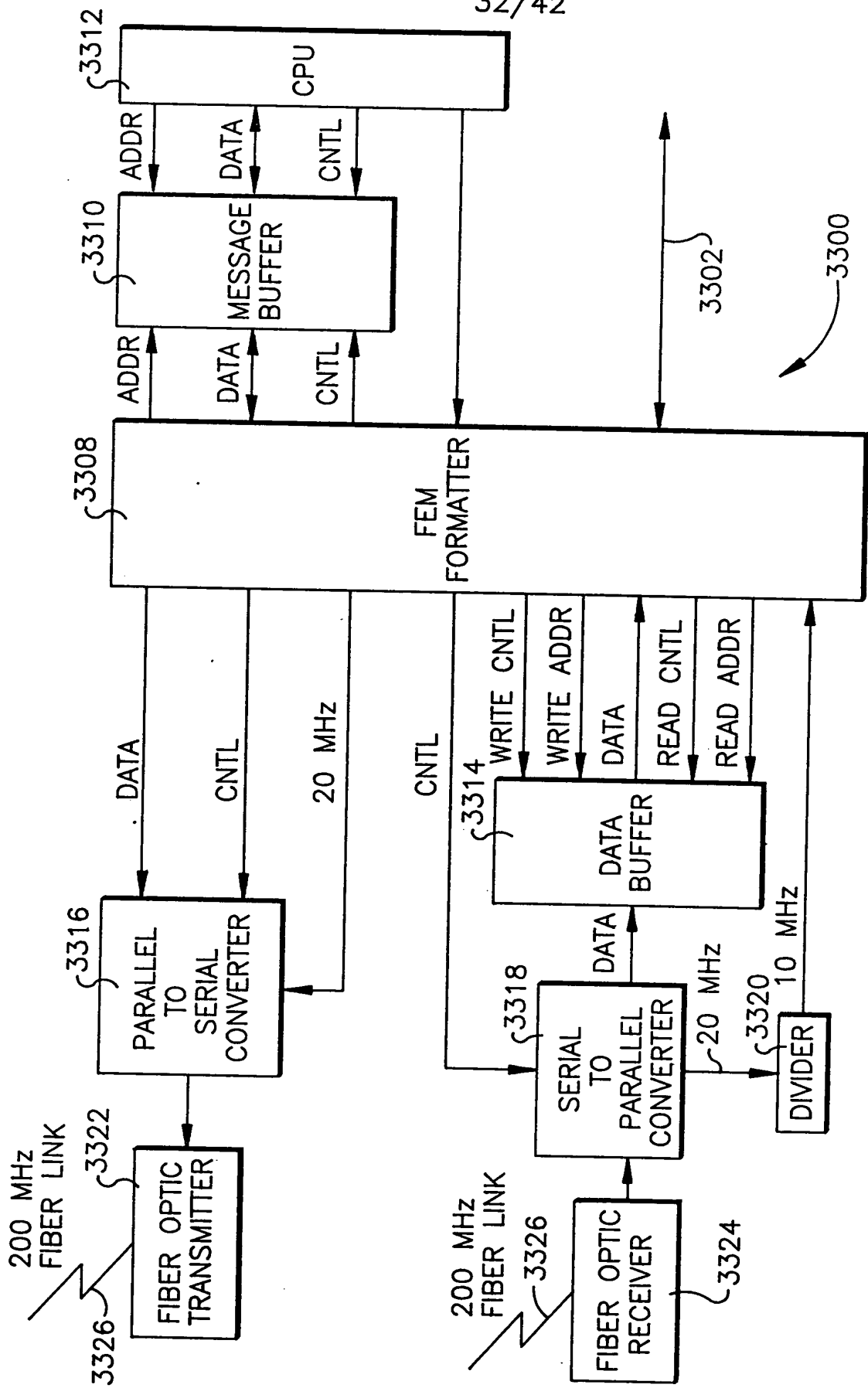
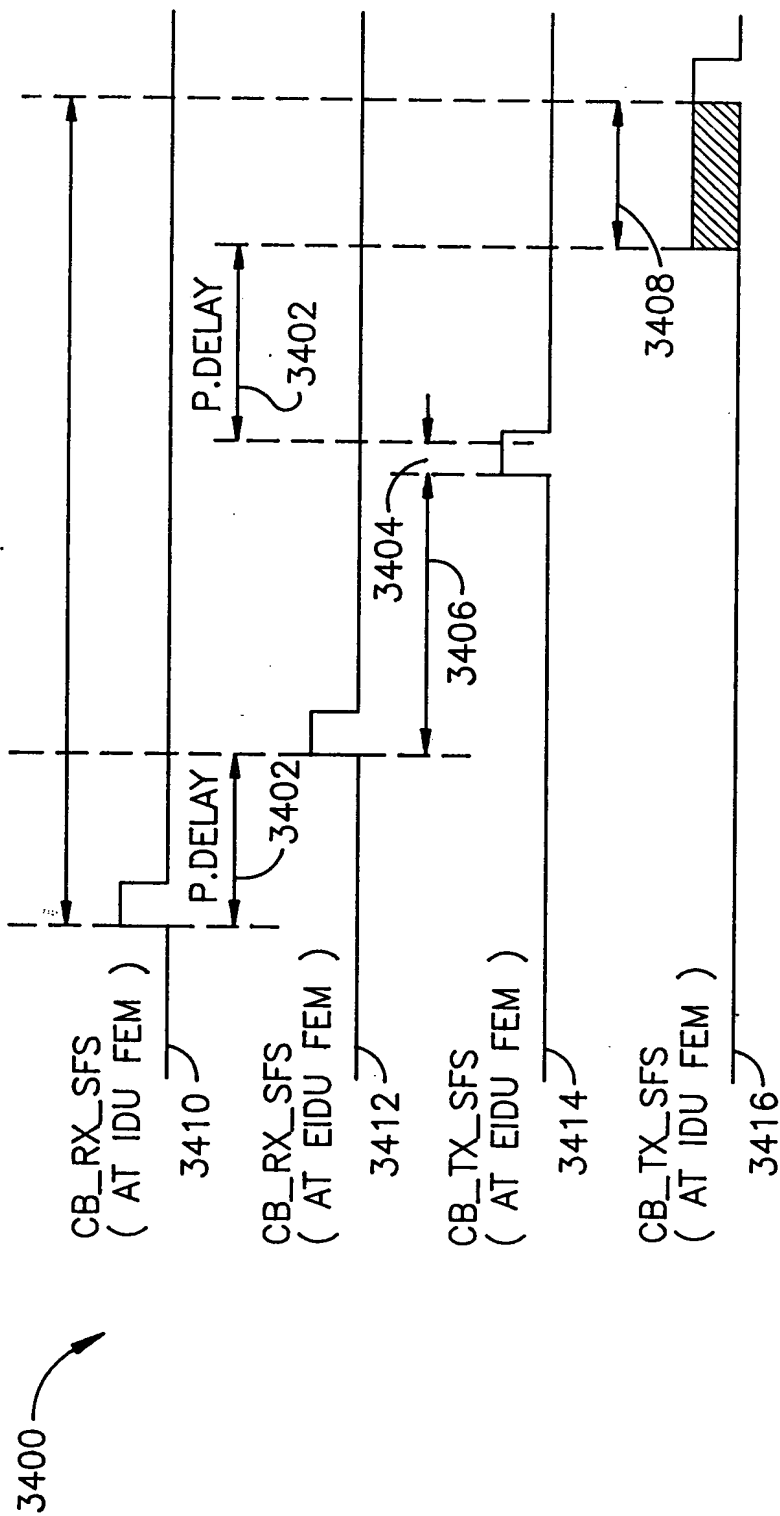
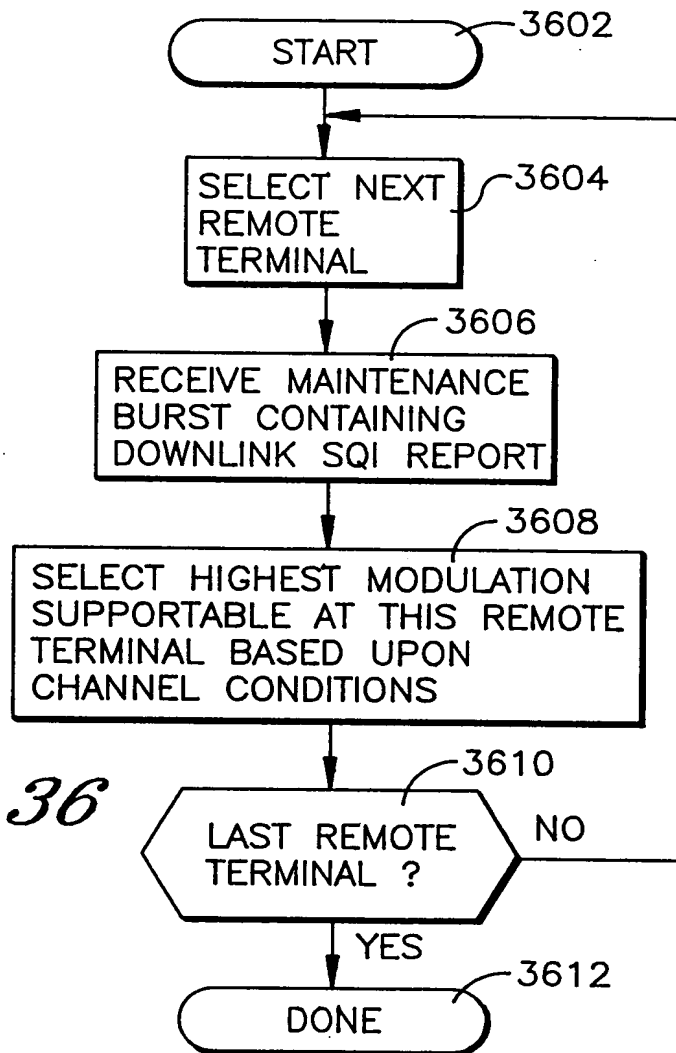


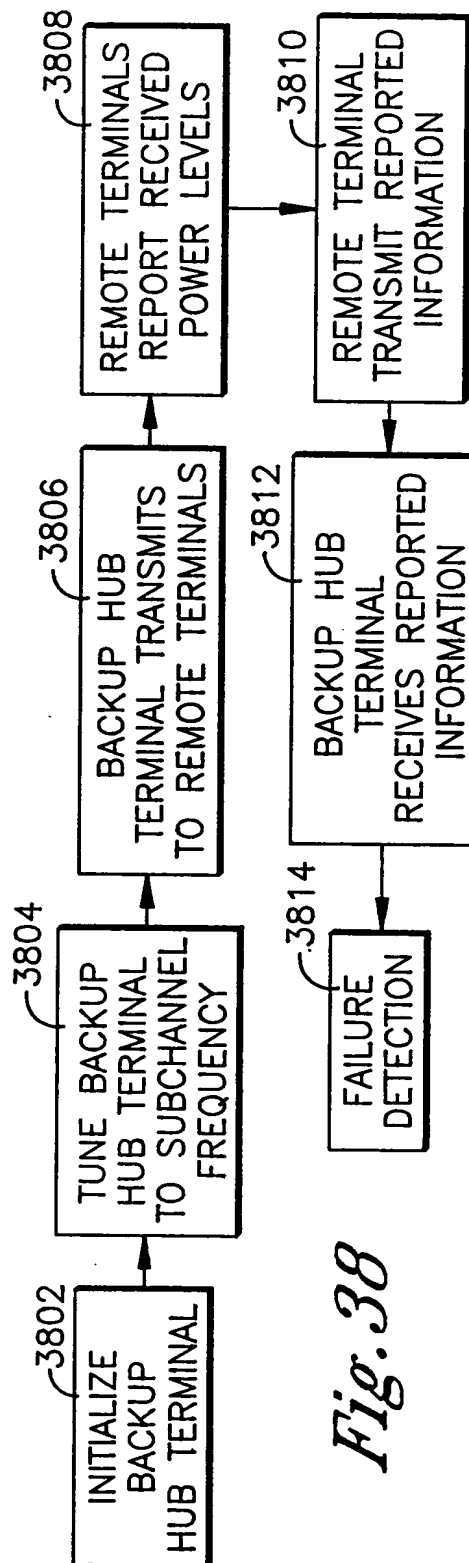
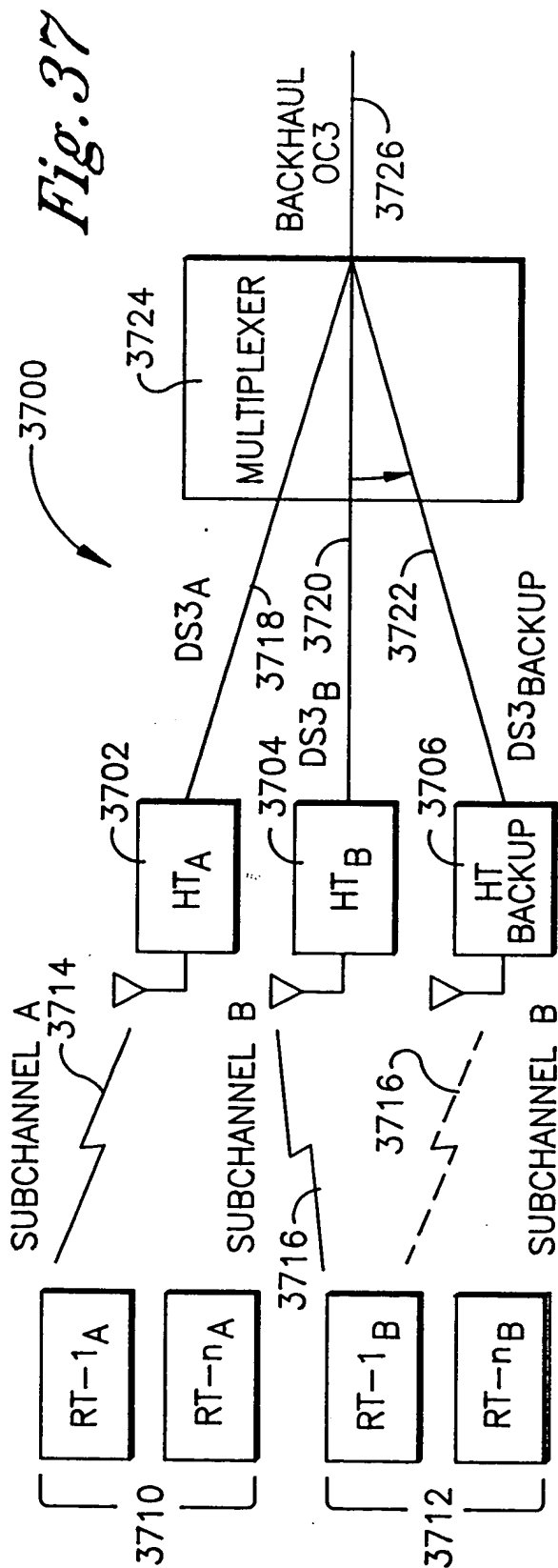
Fig. 33



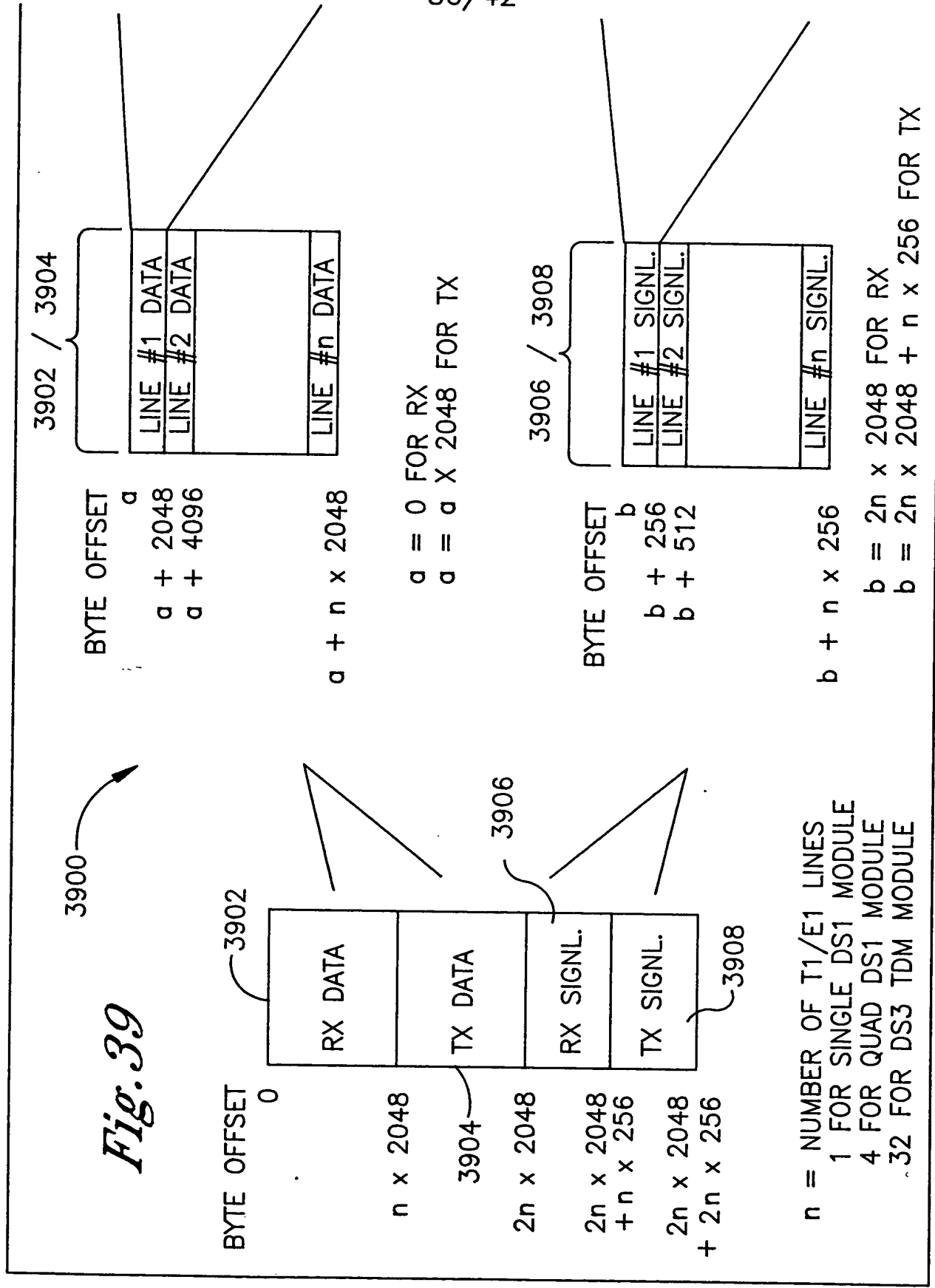


*Fig. 34*

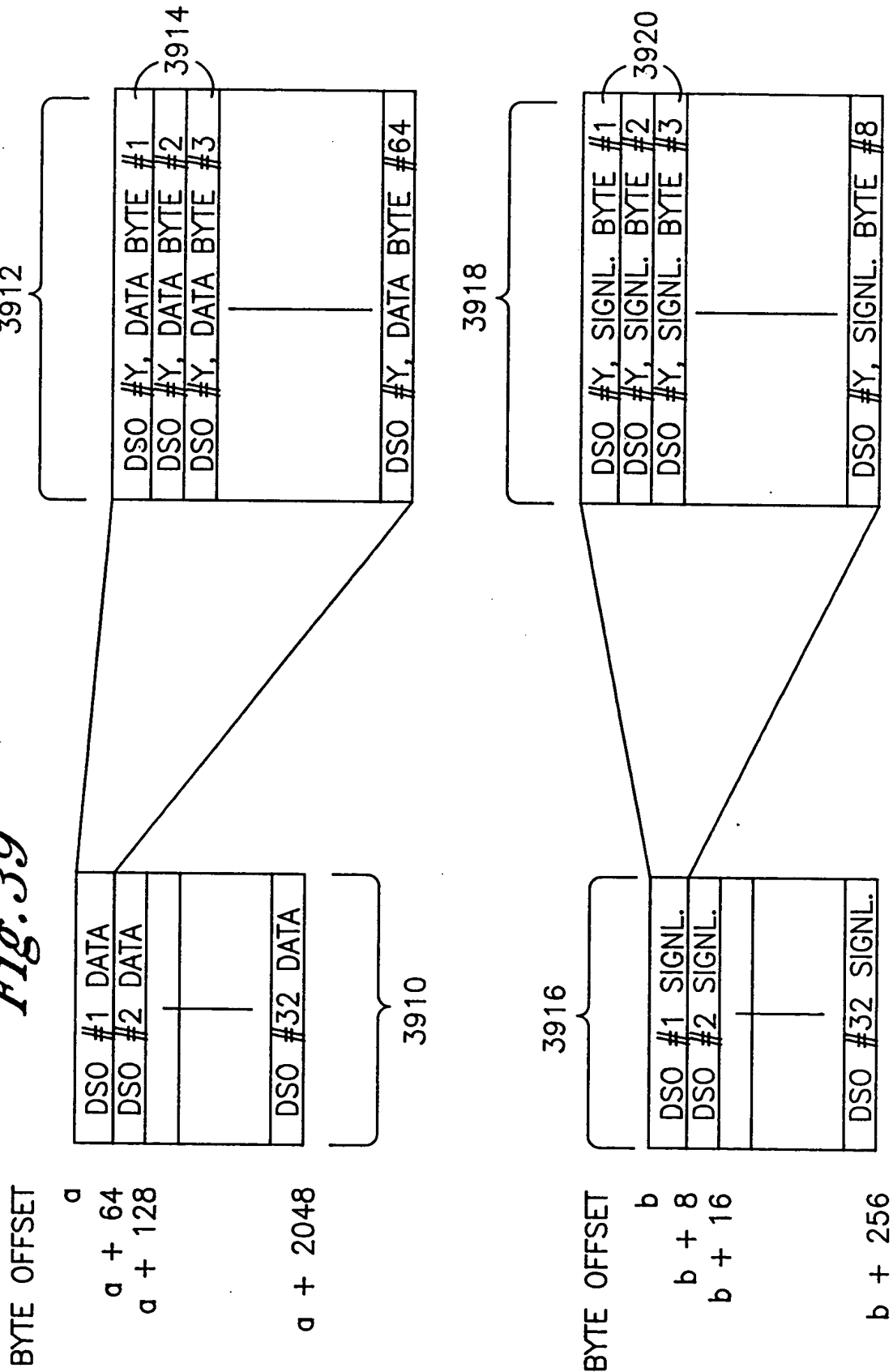
*Fig. 36*



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*Fig. 39*



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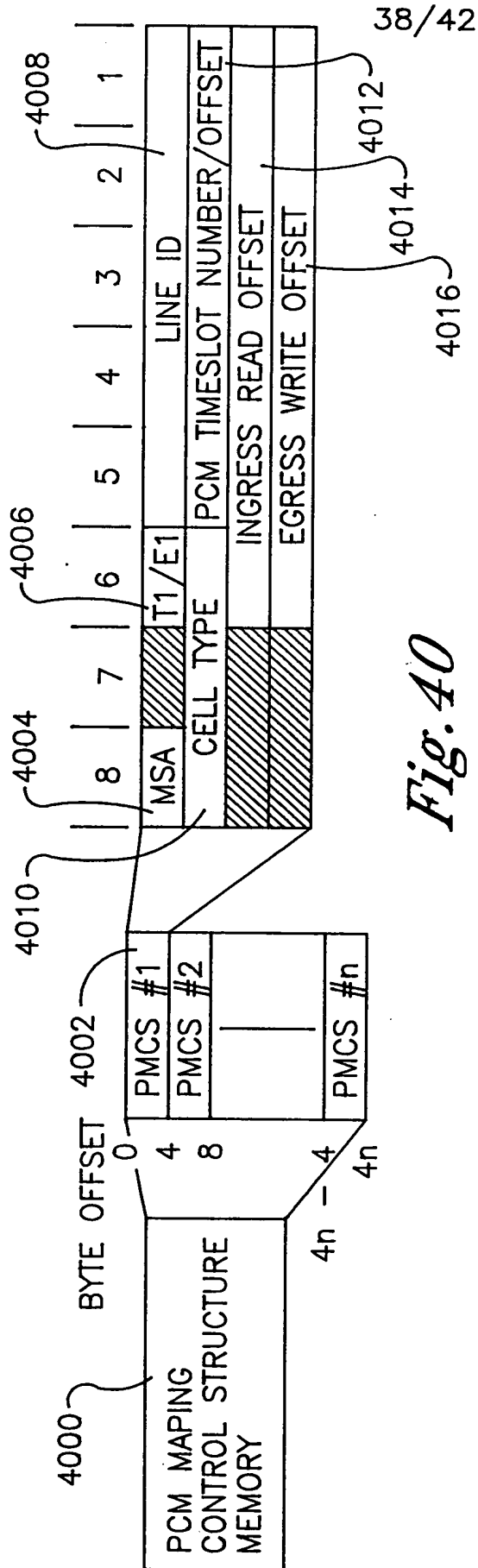


Fig. 40

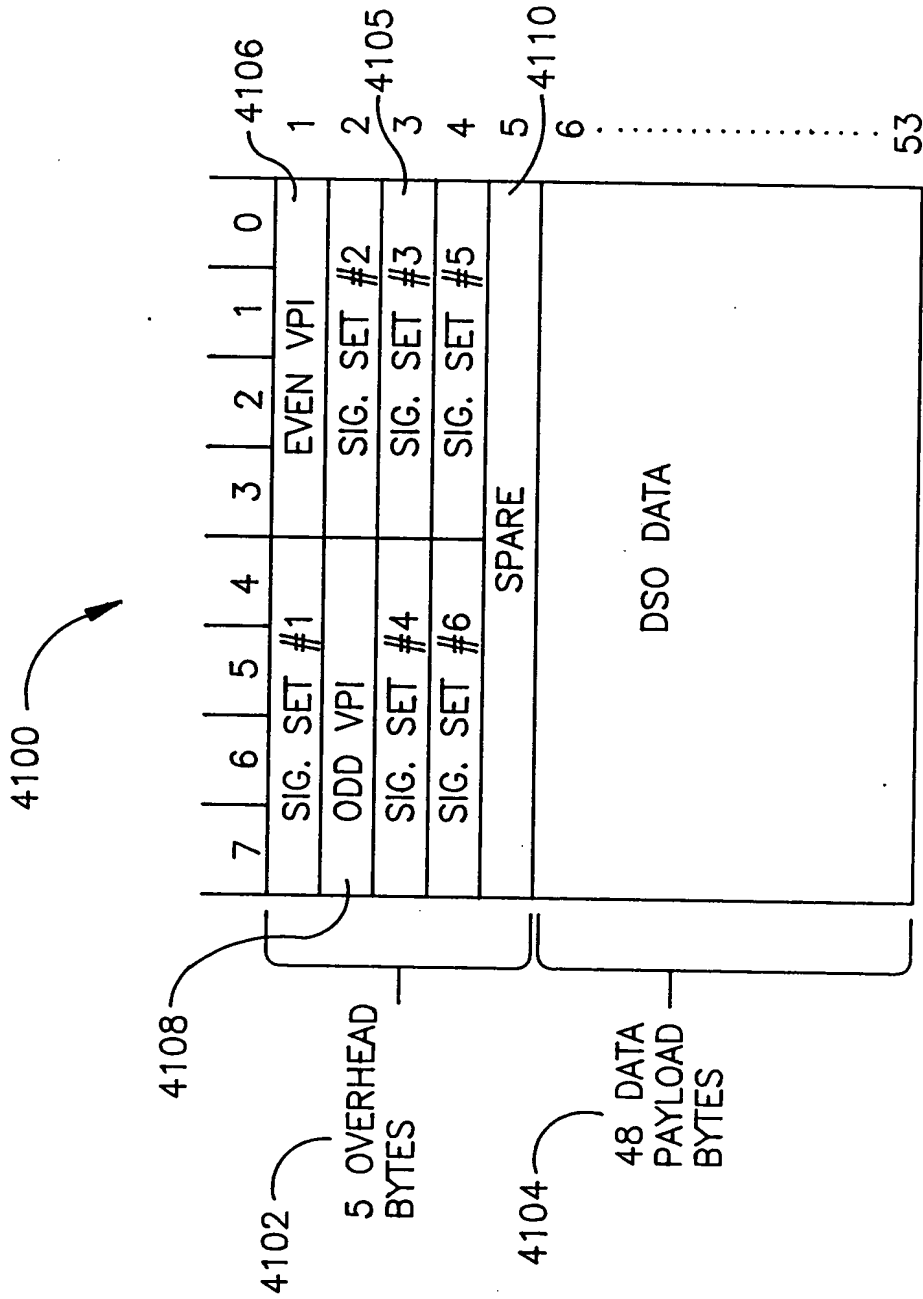
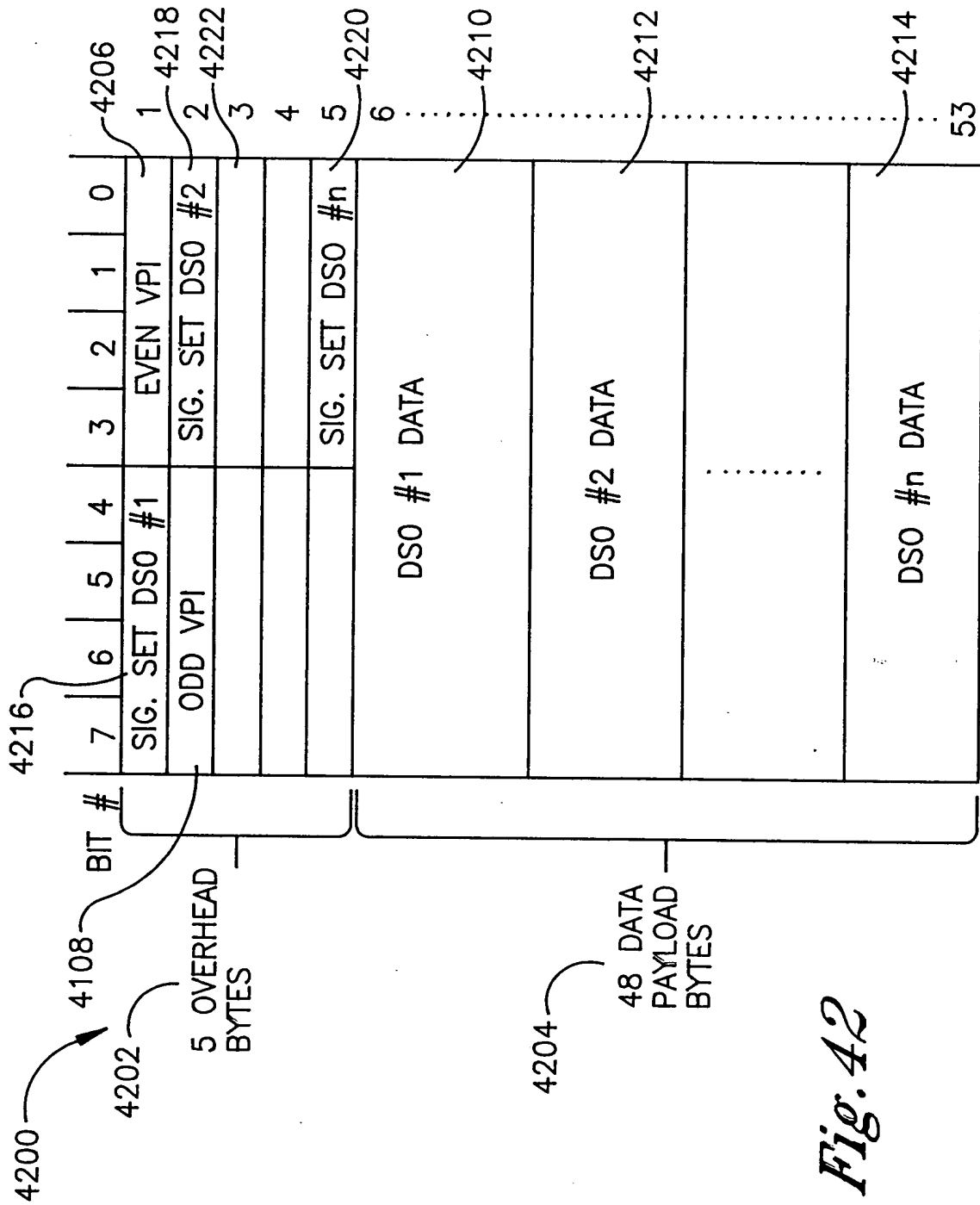


Fig. 41





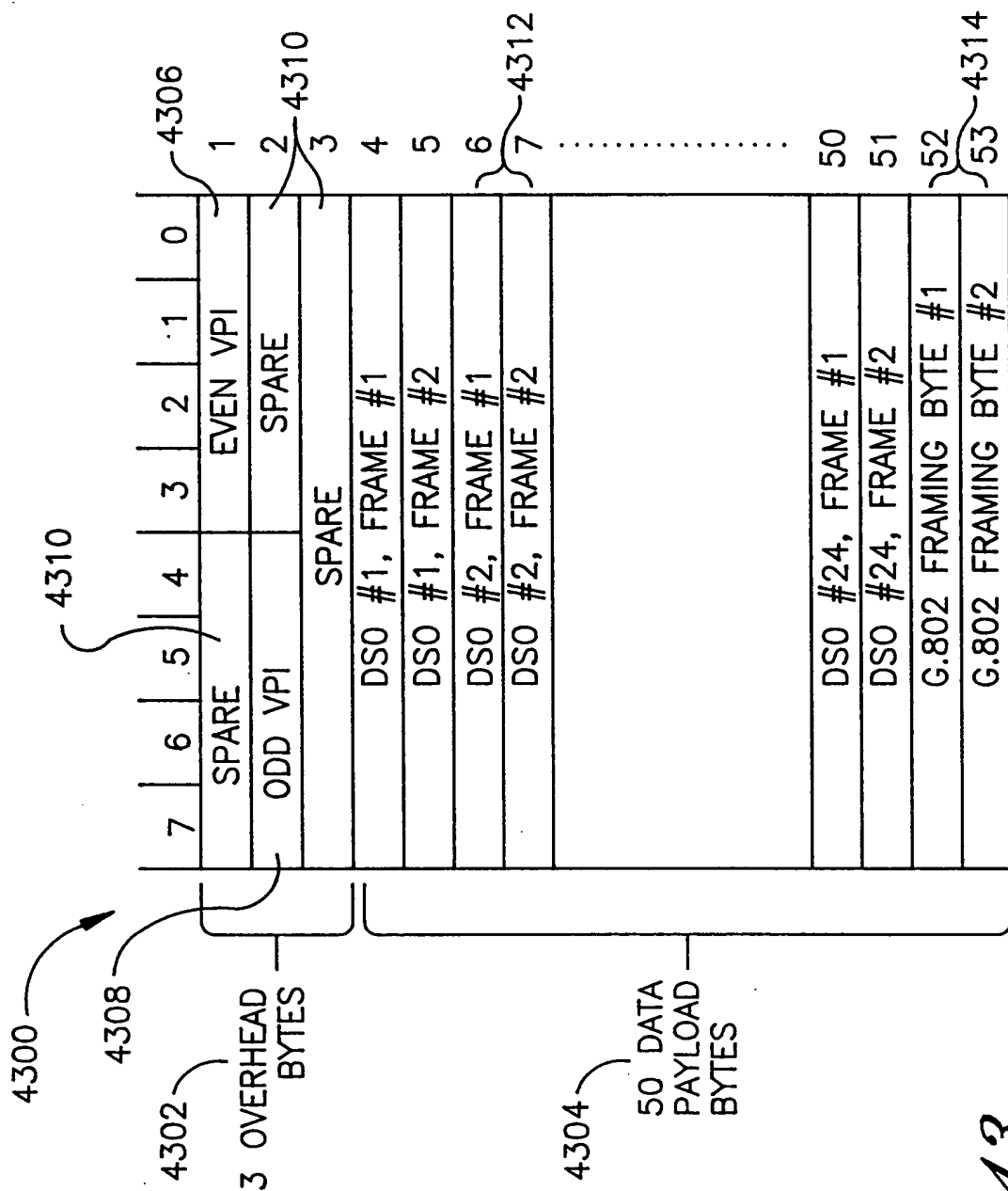
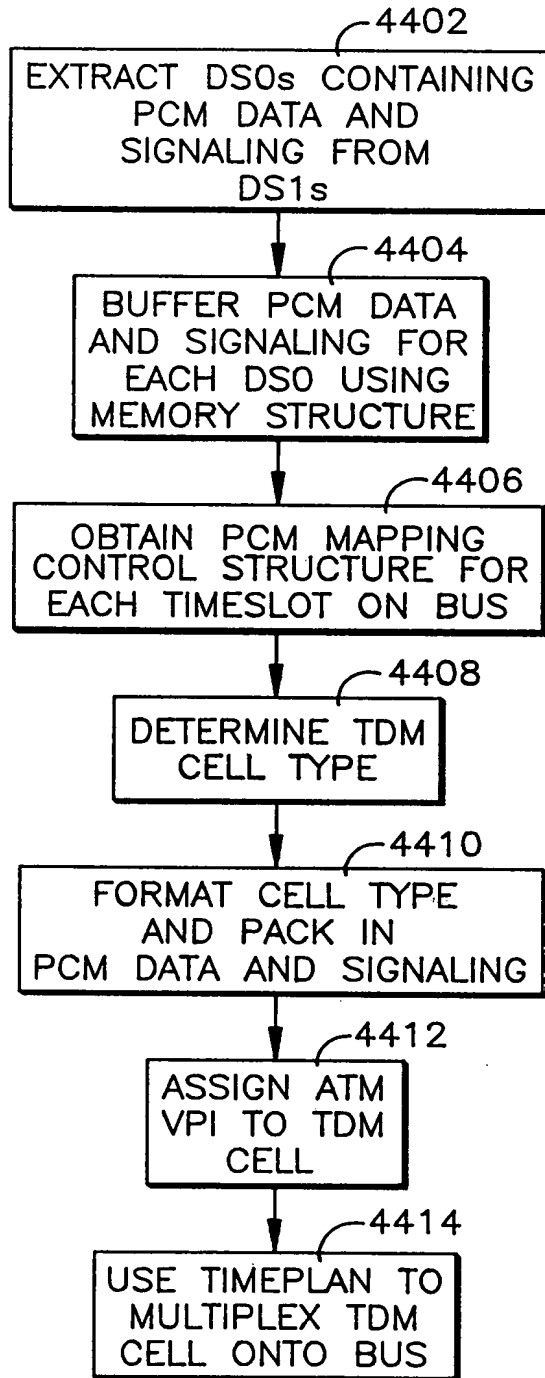
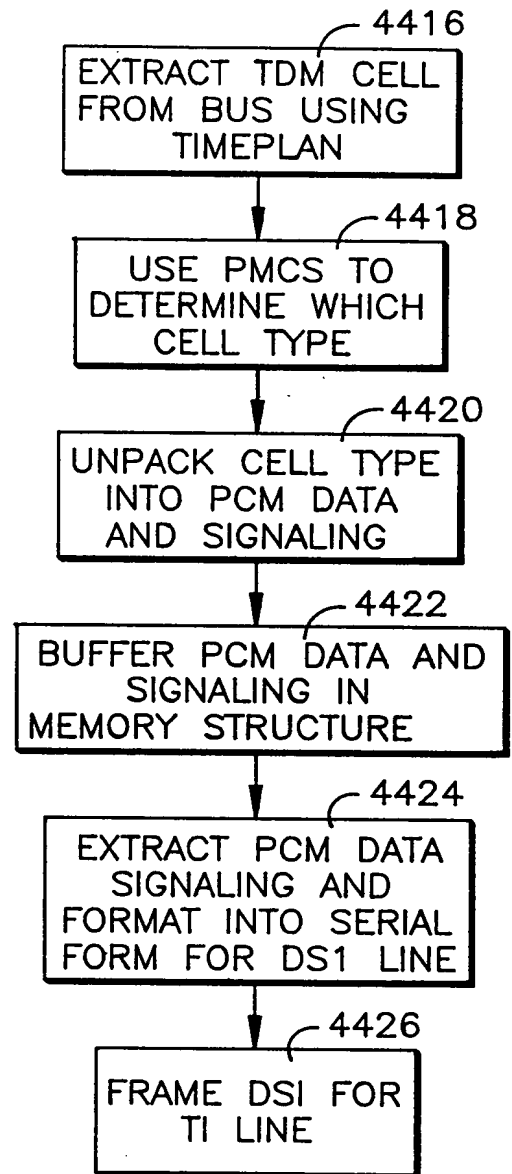


Fig. 43

*Fig. 44A**Fig. 44B*